ZR736342
ZR36060 Reference Design Board

Technical Reference Manual

July 17, 1997

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ZR636342-DM-1.1

ZR36060 Reference Design Board, Technical Reference Manual Rev 1.1, 1997.

Table of Contents

1. Introduction

1.1 Overview

The ZR36060 is a low cost, highly integrated JPEG codec. Its targeted applications are those requiring compression and decompression of motionvideo sequences and still images, at resolutions used in the most popular digital video standards (image width of up to 768 color pixels per line). One common application is in video capture and non-linear editing for the desktop, in which a JPEG add-in board is used with the appropriate drivers to perform Motion JPEG video capture to disk, and acceleration of the compression and decompression operations required by the video editing application software. The reference design described herein is the lowest cost version of such an add-in board. Because of the hardware JPEG compression and decompression, and the efficient interface to the PCI bus, it provides full motion, full resolution capture and playback in PCI systems without taxing the system CPU.

1.2 Data Flow

In motion video capture, the video input of the board is driven by a live video source such as Video Camera, VCR, LD etc. The video can simultaneously be displayed on an external TV monitor and on the PC system's graphics monitor, and can be compressed and transferred to the system memory and from there to the disk. If required, audio is simultaneously captured by means of a standard PC sound card. Synchronization of the audio and video is done by software (in the case of the capture driver supplied with the reference design, by the Video For Windows system software).

In motion video playback, the compressed video stream is transferred to the board from the system memory. The video is decompressed and simultaneously displayed on an external TV monitor as well as on the system PC monitor. The audio stream is played back through the PC sound card. Synchronization is mantained by the Video For Windows system software.

The board accelerates compression and decompression of still images, to support video editing application software. The drivers of the reference design are compatible with Video For Windows (VfW).

1.3 Key Features

- NTSC/PAL CCIR resolution video cpture and playback.
- Motion JPEG compression and decompression.
- High quality scalable video in a window with full graphics overlay support.
- Composite and S-Video analog input/output.
- PCI 2.1 compatibility.
- Plug & Play installation support.

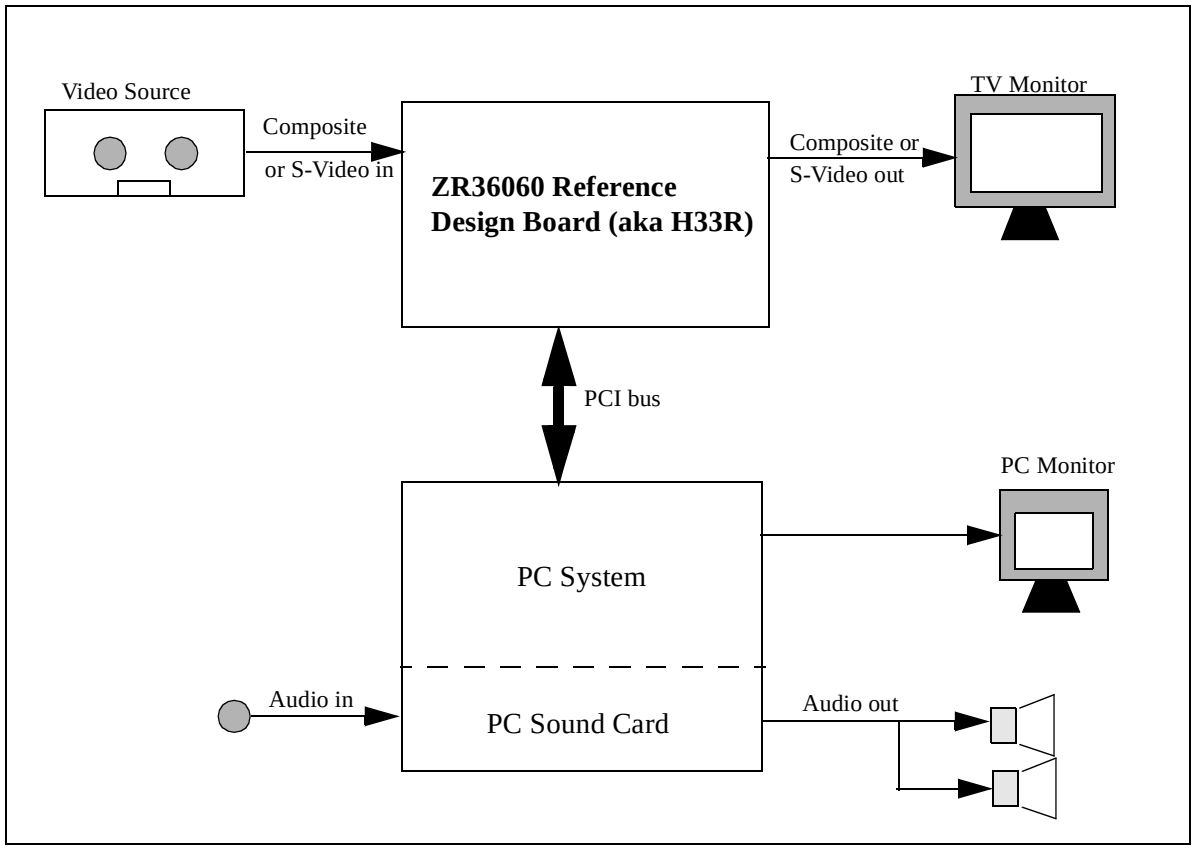
1.4 System Requirements

- A PC system (486 and above) with a PCI bus connector.
- A PCI graphics accelerator that supports linear addressing.
- A PC sound card to support audio capture and playback.
- Windows 95 operating system with Video For Windows run time support installed.
- A live video/audio source (Camera, VCR, LD etc.).
- A TV monitor.

1.5 System Environment

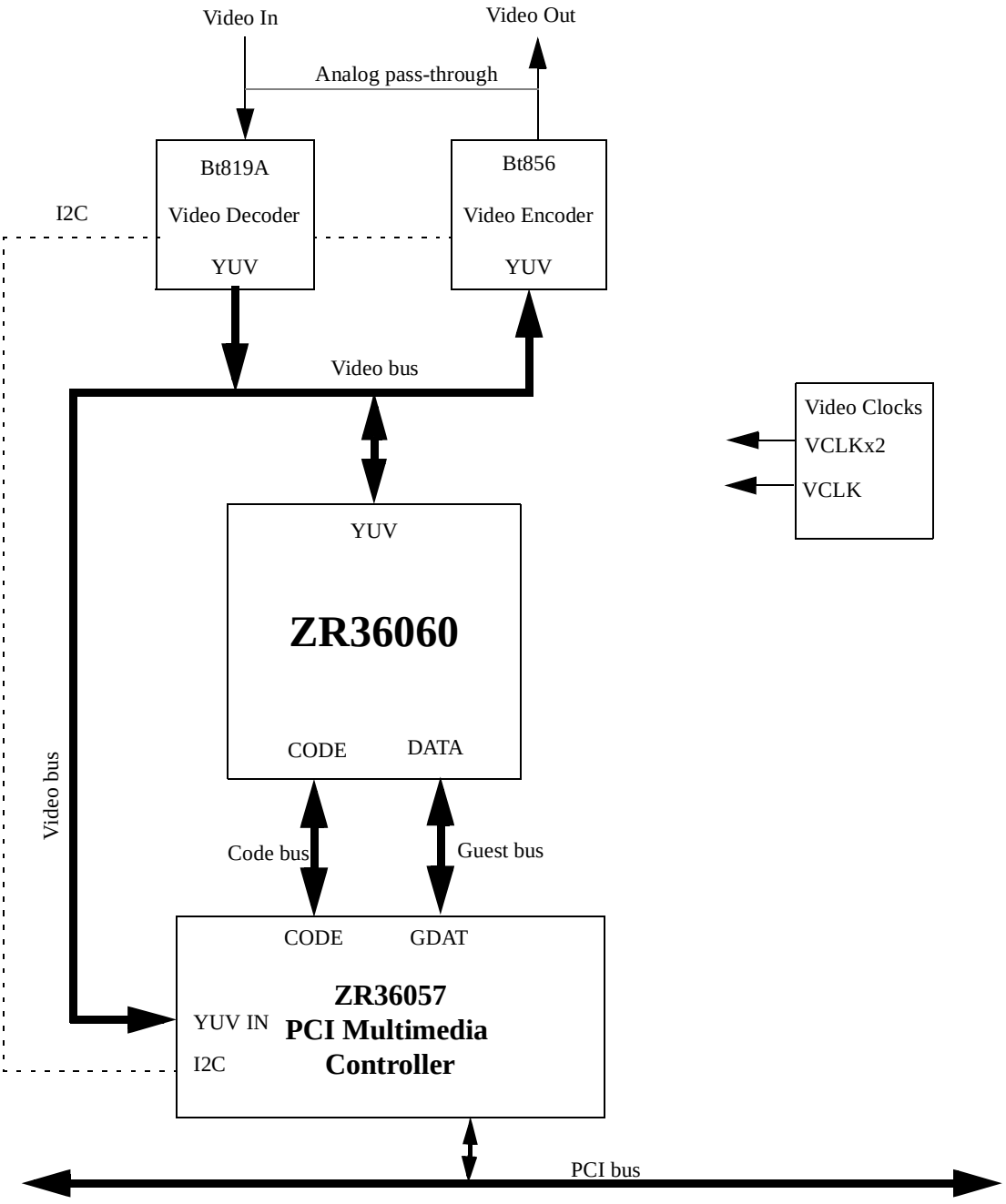
Figure 1 depicts the system environment.

FIGURE 1. System Environment



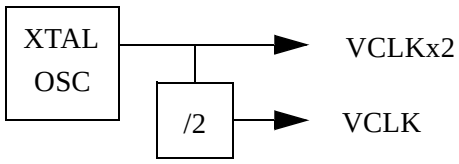
2. Functional Description

FIGURE 2. Basic block diagram



2.1 Video Clock Generator

FIGURE 3. Video clock generator



A stable video clock (from a crystal oscillator) is fed to the output fifo stage of the Bt819A video decoder, and to the video encoder in playback mode. This clock source gives a high accuracy, high quality, zero-jitter system, as compared with PLL based video systems. The oscillator (producing the VCLKx2 signal) is 27.0000Mhz for CCIR sampling rate (both PAL and NTSC). This signal is fed into a 74F74 DFF device to divide the frequency by 2 and create the VCLK signal.

To permit correct operation of the ZR36057 to see ‘video-in-a-window’ the Bt819A decoder is operated in API mode, for continuous pixel stream.

2.2 Video Decoder - Bt819A

The Video Decoder digitizes the incoming video in CCIR-601 format and generates the video sync signals.

The analog VIDEO_IN is also passed through to the VIDEO_OUT connector for TV display of live video while capturing, via the QS3257 analog switch device.

The digital YUV 4:2:2 video is simultaneously captured by the ZR36060 for JPEG compression and the ZR36057 for PC video overlay. During decompression the video bus of the video decoder is disabled, to allow for the ZR36060 video output.

Host control of the Bt819A is performed by the ZR36057 I2C port. Parameters like Brightness/Contrast/Hue can be adjusted by the user.

2.3 Video Encoder - Bt856

The encoder, used only during decompression, interfaces to the YUV 4:2:2 digital bus of the ZR36060, converts to analog and outputs a composite or S-video output (selectable via *SVideo#* host control), that can be displayed on a NTSC or PAL monitor according to the desired video standard.

The host control of the encoder is performed by the ZR36057 I2C port.

2.4 JPEG Codec - ZR36060

The ZR36060 compresses and decompress images, in YUV 4:2:2 video format only, using the JPEG baseline method. During compression, video from the Bt819A present on the video bus is sampled at the YUV port of the ZR36060. The compressed code is output via the Code port of the ZR36060, and sent via the ZR36057 controller to the systems's main memory. In decompression the coded compressed video is fetched from main memory by the ZR36057, sent to the ZR36060 via the Code port, expanded according to the JPEG standard and output to the video encoder and the ZR36057's video port (for video-in-a-window display).

A dedicated 3.3V power supply is needed to operate the ZR36060, and is implemented with a 5V -> 3.3V linear voltage regulator. The PCI +3.3V rail is not used, since this is an optional feature, frequently not available in PC systems.

In normal operation the ZR36060 Code interface is operated at its maximum transfer rate: Master mode, CFIS=0 (one clock per transfer cycle).

The ZR36060 host control is performed by the ZR36057 *GuestBus* port:

- Access to the 1K internal registers array is done via Guest #0.
- START# operation (activate beginning of compression/decompression process) is done via Guest #1.
- RESET# to the ZR36060 is accomplished via a dedicated Guest #3 line, to permit recovery from stuck situations without reseting the complete video path.

2.5 Multimedia Adapter - ZR36057

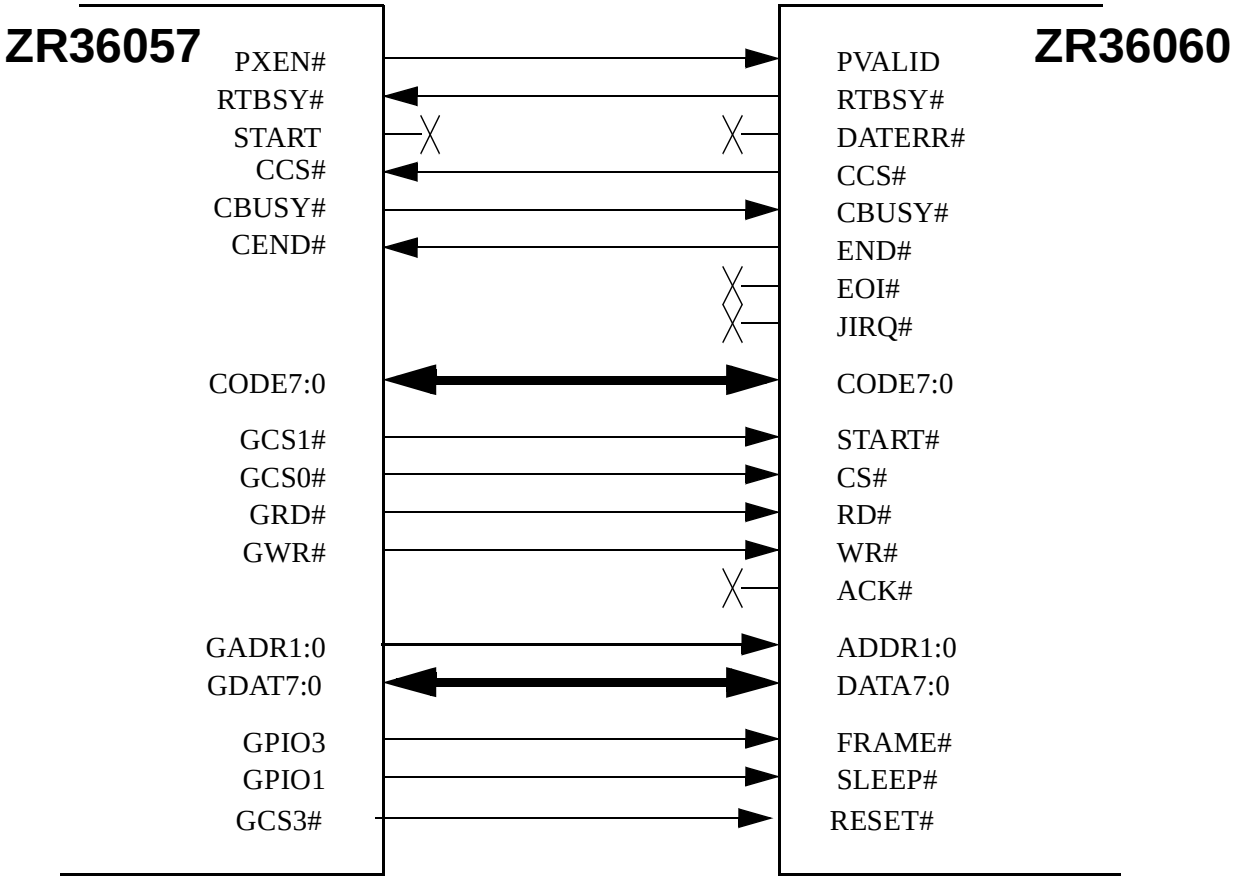
The ZR36057 is the PCI bridge and the main process controller of the board. The ZR36057 interfaces to the video bus. The incoming video is optionally scaled down and converted into RGB format. The processed video can be transferred with full overlay support directly to the graphics display memory, or to main system memory, using PCI bus mastering.

Coded video is transferred via the ZR36057 to or from the system memory using PCI bus mastering. The ZR36057 interfaces to the host and the ZR36060 in order to perform still image compression and decompression. The image pixels are transferred one by one using a dedicated "Still Transfer" mechanism.

The ZR36057 bridges the host CPU accesses to ZR36060. Using a handshake mechanism (*PostOffice*), the host accesses to an ZR36057 internal register are reflected to the ZR36057's *GuestBus*. See Appendix A for the Guest Bus mapping.

The ZR36057 controls several board features by means of its GPIO pins. See Appendix A for the mapping. Since the GPIO pins float until the ZR36057 is configured, default values during power-up and initialization are obtained with the use of pullup/pulldown resistors on the board.

FIGURE 4. Interconnection of ZR36057 and ZR36060



3. Power Budget

The maximum current consumption from the +5V PCI rail is 1.4A. This gives a maximum power consumption of 7W.

The supply for the analog circuits (video decoder and encoder) can be brought from the same +5V PCI rail as the digital circuits. The image quality is not degraded by doing this, thus it saves the use of additional components such as a voltage regulator and heatsink.

Following the PCI specification, the board supports the PRSNT1# and PRSNT2# settings, to give the host system power consumption information. Based on the maximum power consumption the PRSNT1:2# == GND.

4. Modes of Operation

The board supports four basic modes of operation:

- Motion Capture and Compression.
- Motion Decompression and Playback
- Still Image Compression.
- Still Image Decompression.

The board data flow in each of the modes is described in the following sub-sections and corresponding figures.

4.1 Motion Capture and Compression

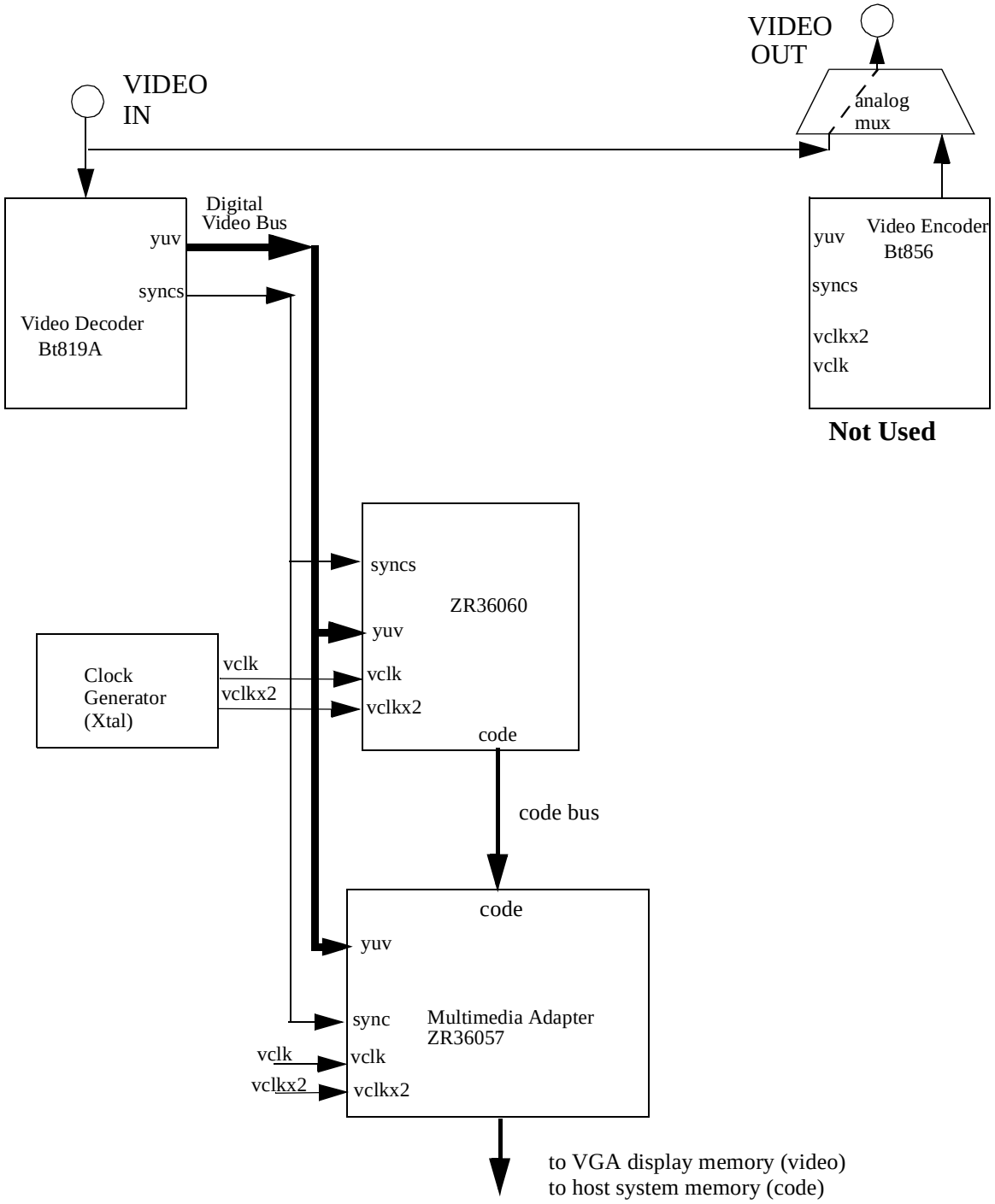
The Video Decoder (Bt819A) samples the analog video input and drives the video in YUV 4:2:2 format onto the video data and syncs bus.

The analog video is passed through to the video out connector, to monitor the capture on the TV monitor, using the video mux. The digital video stream and the sync signals are directed simultaneously to:

- The video port of the ZR36060 for JPEG compression.
- The video port of the ZR36057 to be optionally scaled down, converted to RGB format and transferred via the PCI to the PC graphic display.

The ZR36060 compresses the active video rectangle of the field, and transfers the coded stream to the ZR36057 using Code Master mode and CFIS = 0. The ZR36057 drives the code, using PCI DMA, to an allocated system memory buffer.

FIGURE 5. Motion Capture And Compression Flow



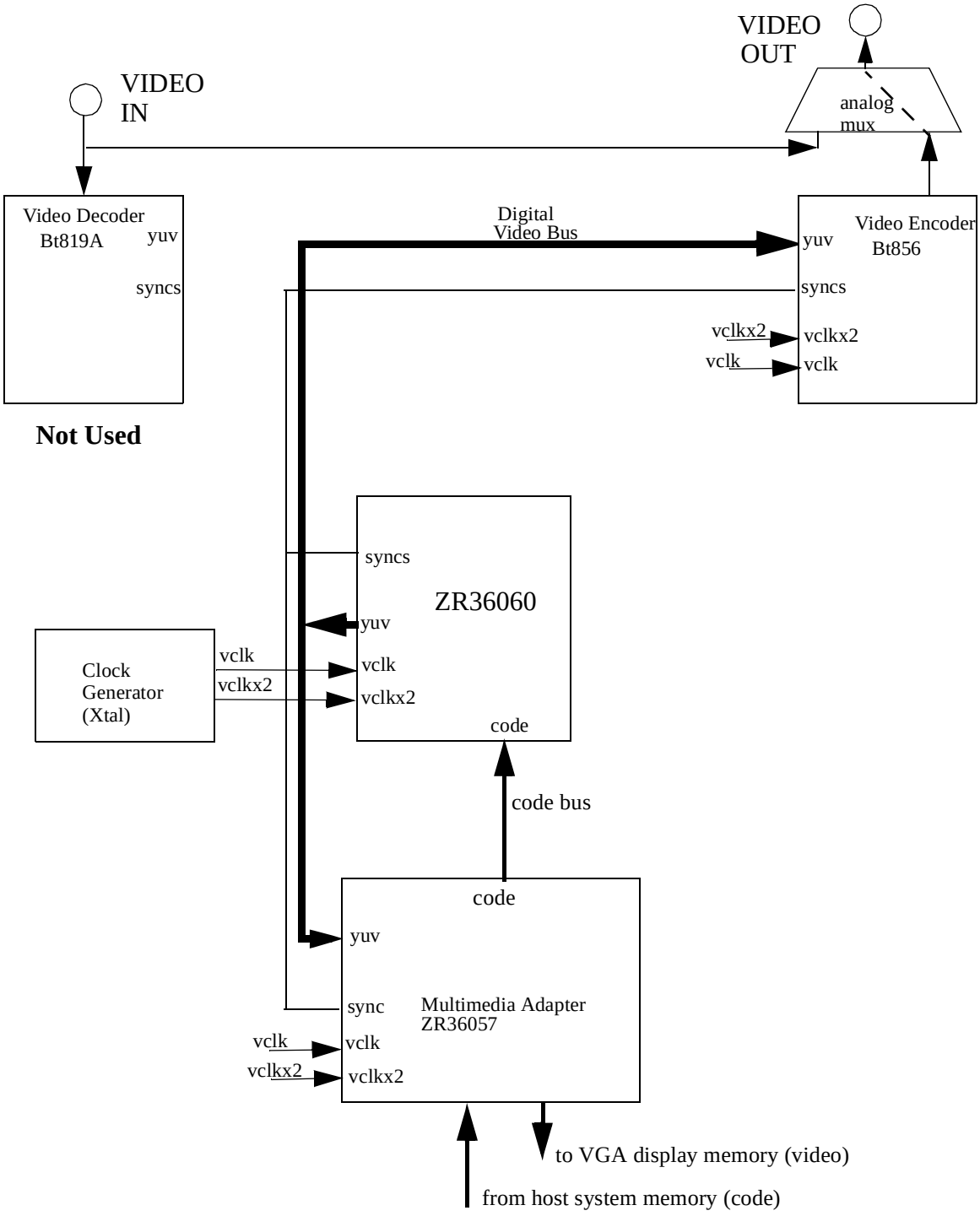
4.2 Motion Decompression and Playback

The ZR36057 transfers the code using PCI DMA from the system memory, and drives the code stream via the Code Bus to the ZR36060 in code master mode with CFIS = 0.

The ZR36060 drives the decompressed pixels (in the programmed active area) to the video bus. The video sync signals can be provided either by the video encoder, the ZR36060, or the ZR36057 operating as a sync master. The video output bus and syncs of the Bt819A are floated by software control in order to prevent bus contention. The video stream and sync signals are directed simultaneously to:

- The video encoder to drive the analog video output for display on a TV monitor.
- The video input of the ZR36057 to be optionally scaled down, converted to RGB format and transferred via the PCI bus to the PC graphics display.

FIGURE 6. Motion Decompression and Playback Flow



4.3 Still Image Compression

Still image compression is used by video editing application software, to compress an imported bitmap image, or recompress a bitmap image expanded from a captured JPEG sequence after adding special effects. The bitmaps are in RGB format, usually 24, 16 or 15-bit pixel depth.

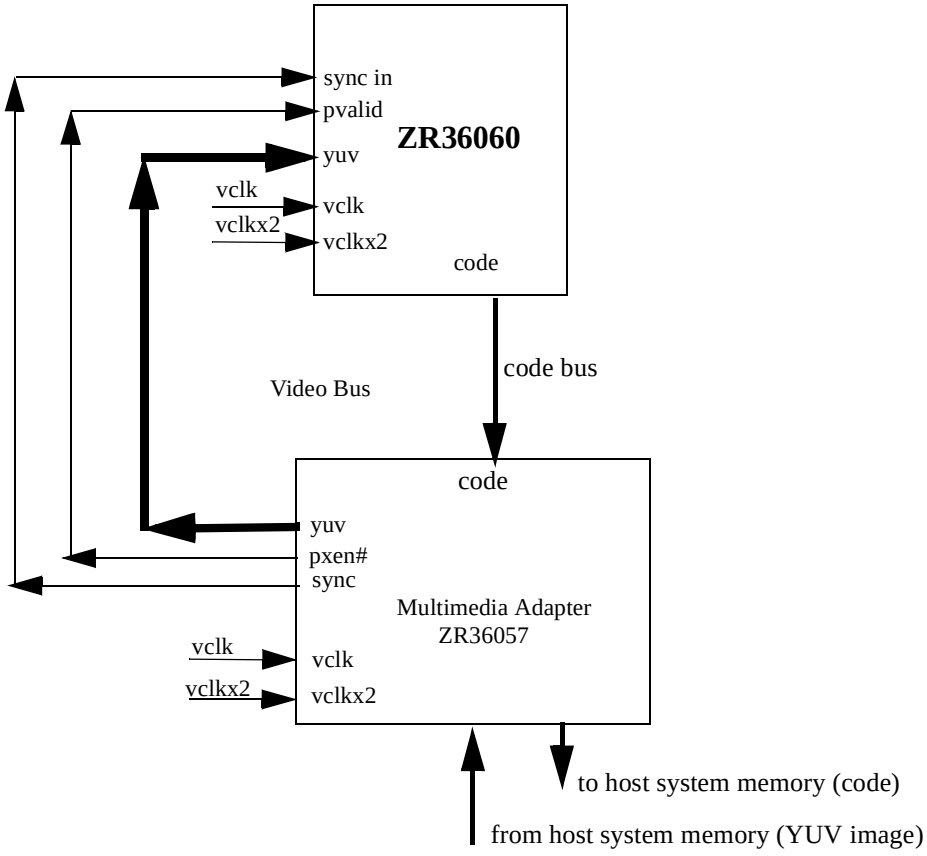
The board does not include a color space converter, besides the one in the ZR36057 for the video-in-a-window path to the PC monitor. Therefore, before the actual compression of the image takes place, it must be transformed by software from the RGB color space to YUV.

After color space conversion, the host CPU uses the ZR36057's dedicated Still Transfer mechanism to transfer the image from the system memory. The host CPU writes the image, pixel by pixel, already in YUV format, to the ZR36057's video port register.

The ZR36057 operates the video sync signals and drives the ZR36060 video port using the PXEN# (PVALID) signal on a pixel by pixel basis. The Bt819A video output and sync signals are floated by the software. Also, the video encoder is disabled in this mode, since the pixel flow on the video bus slow-speed, not real time video.

The ZR36060 compresses the video stream and transfers the compressed field to the ZR36057 using Code Bus master mode. The ZR36057 drives the code, using PCI DMA, to an allocated system memory buffer.

FIGURE 7. Still Image Compression Flow



4.4 Still Image Decompression

Still image decompression is used by video editing applications to decompress a single frame from a JPEG sequence to an RGB image bitmap, before applying special effects.

The ZR36057 transfers the code using PCI DMA from the system memory. The code stream is fetched via the Code Bus by the ZR36060 operating in Code Master mode.

Still image decompression has the same data flow as Motion Decompression, with the difference that the decompressed image is fed to an allocated image buffer in the system memory instead of the graphics display memory. This is accomplished using the frame grabbing option of the ZR36057.

Us of the same path as motion decompression implies that no host intervention is involved in the image data transfer. This is to be contrasted with still image compression, in which the host software is heavily involved, having to transfer the image pixel by pixel interactively to the ZR36057. There is also no need for the software to perform color space conversion, since the ZR36057 performs the desired YUV -> RGB conversion in its built-in video path.

Appendix A

ZR36057 GPIO Mapping

	31	30	29	28	27	26	25	24
0x02C	*FRST#*	X	*VidOut*	X	*Frame#*	*SVideo#*	*JSleep#*	*Reset#*
type	OUT		OUT		OUT	OUT	OUT	OUT
default	X	X	0	X	1	1	1	0

Reset# Main hardware reset for Video Decoder and Encoder devices
- 0 - Assert RESET# line
- 1 - Deassert RESET#. Normal operation.

JSleep# SLEEP# input of ZR36060. Used for initial clock frequency locking and to place the ZR36060 in power-down mode.
- 0 - ZR36060 enter SLEEP mode.
- 1 - ZR36060 PLL locks to the video clock and returns to normal operation.

SVideo# Selects output mode of video encoder Bt856. The analog video input/output modes must be the same, that is, if video in is composite, then video out must be composite too, and if video in is S-video, then video out must be S-video.
- 0 - Analog video output is S-video
- 1 - Analog video output is composite video

Frame# FRAME# input of ZR36060. Used to synchronize the START of process on the next odd VSYNC. If continuously asserted, the ZR36060 performs temporal decimation, processing odd fields only.
- 0 - FRAME# asserted; Start on next odd VSYNC.
- 1 - FRAME# deasserted; Start on next VSYNC, whether even or odd.

VidOut Video Output Select (analog mux control).
- 0 - Selects Video In -> Video Out analog pass through (used in Capture)
- 1 - Selects Video Out from Bt856 encoder (used in Playback)

FRST# Video Decoder FIFO Reset. Must be toggled every init of the Bt819 device:
- 0 - Reset the internal FIFO while initializing the device.
- 1 - Normal operation.

ZR36057 Guest Bus Mapping

Guest #0 - ZR36060 Registers

Tdur/Trec = 12 / 3 PCICLK

	7	6	5	4	3	2	1	0
0x0 R/W	*Code FIFO 7:0 (Slave mode only)*							
0x1 W	*Host Address 9:8*							
0x2 W	*Host Address 7:0*							
0x3 R/W	*Host Data 7:0*							

See ZR36060 data sheet for explanation of these 4 registers

Guest #1 - ZR36060 START# signal

Tdur/Trec = 12 / 3 PCICLK

	7	6	5	4	3	2	1	0
0x0 W	*START#*							

Guest #3 - ZR36060 RESET# signal

Tdur/Trec = 12 / 3 PCICLK

	7	6	5	4	3	2	1	0
0x0 W	*RESET#*							

Appendix B

Bill Of Materials (next two pages)

ZR36060 REFERENCE DESIGN BOARD (H33R) REV.1.0							
Item	**Qty**	**Reference**	**Value**	**Description**	**Package**	**Manufacturer**	**Comments /**
			& Part Number				**Assembly Comments**
1	2	CON1,CON2	S-VHS	4pin female miniDIN conn.	90-TH	Any	
			MD40SM			CUI	
2	61	C1,C2,C3,C4,C5,C6,C7,C8,	0.1UF (100nF)	Cer. Cap.	SMD-0805	Any	
		C9,C10,C11,C12,C13,C14,					
		C15,C16,C17,C18,C19,C20,					
		C21,C22,C23,C24,C27,C28,					
		C29,C30,C31,C32,C34,C35,					
		C36,C37,C38,C40,C41,C42,					
		C43,C44,C45,C47,C48,C49,					
		C57,C58,C59,C60,C67,C68,					
		C71,C72,C78,C80,C83,C84,					
		C87,C88,C89,C90,C94					
3	8	C25,C33,C85,C86,C91,C92,C93	47UF 16V	Tan. Cap.	SMD-C\D	Any	
4	4	C61,C66,C74,C76	22PF	Cer. Cap.	SMD-0805	Any	**C61,C66 - NC**
5	2	C62,C65	270PF	Cer. Cap.	SMD-0805	Any	
6	4	C63,C64,C75,C77	330PF	Cer. Cap.	SMD-0805	Any	
7	2	C69,C70	33PF	Cer. Cap.	SMD-0805	Any	
8	4	C73,C79,C81,C82	390PF	Cer. Cap.	SMD-0805	Any	
9	4	FB1,FB2,FB3,FB4	80R @ 100MHz, 500mA	Ferrite bead	5mm,TH, Vertical (Radial)	Any	
			BL02RN1-R62T2-01			Murata	
10	2	J1,J2		RCA Jack	90-TH	Any	
			LPR6520-08XX			SMK	
11	2	L1,L2	1.8UH	Inducator	SMD-1812/1210	Any	
12	2	L3,L4	3.3UH	Inducator	SMD-1812/1210	Any	
13	1	L5	2.2UH	Inducator	SMD-1812/1210	Any	
14	1	L6	2.7UH	Inducator	SMD-1812/1210	Any	
15	2	OSC1,OSC2	27.0000MHZ	50 ppm TTL Clk. Osc.	TH-8/14 DIP (300mil)	Any	**OSC2 - NC**
16	6	RN1,RN2,RN3,RN5,RN6,RN7	8*10K	8 x 10K Bussed net res.	9-SIP, TH	Any	
			4609X-101-103			Bourns	
17	1	R1	71R5 1%	Res.	SMD-0805	Any	
18	2	R2,R3	75R 1%	Res.	SMD-0805	Any	
19	3	R4,R5,R9	1M	Res.	SMD-0805	Any	
20	2	R6,R7	30K	Res.	SMD-0805	Any	
21	1	R8	2K	Res.	SMD-0805	Any	
22	7	R12,R13,R14,R23,R31,R32,R34	0R	Res.	SMD-0805	Any	**R32,R31- NC**
23	8	R15,R16,R17,R18,R19,R20,	1K	Res.	SMD-0805	Any	
		R21,R22					
24	3	R24,R25,R30	33R	Res.	SMD-0805	Any	
25	2	R26,R29	330R	Res.	SMD-0805	Any	
26	2	R27,R28	220R	Res.	SMD-0805	Any	
27	1	R33	10K	Res.	SMD-0805	Any	
28	4	TP1,TP2,TP3,TP4	1 pin 0.1" Header	Test Point (TP)	TH	Any	**NC**
29	1	U1	BT856KPJ	Video encoder	68 PLCC , SMD	**Brooktree**	
30	1	U2	QS3257	Quad 2:1 Analog mux	SOIC 16 SMD	**Quality Semi**	
31	1	U3	BT819AKPF	Video decoder	100 PQFP	**Brooktree**	
32	1	U4	ZR36060PQC	JPEG processor	100 PQFP	**ZORAN**	
33	1	U5	ZR36057PQC	PCI bus interface	208 PQFP,0.5p, SMD	**ZORAN**	
34	1	U6	LT1117CST-3.3	3.3V/800mA Voltage regulator	SOT-223, SMD	**Linear Tech**	
35	1	U7	74F74D	Dual flip flop	SMD-14-SO (751A-02)	Any	
36	1	Y1	28.6363MHZ	Crystal Osc. +/- 20 PPM	HC49U/S , TH	Any	
37	1	Y2	35.4689MHZ	Crystal Osc. +/- 20 PPM	HC49U/S , TH	Any	
38	1	H33R PCB		6 Layer PCB		**ZORAN**	Gerber files available
39	1	Rear Panel Bracket		Bracket + 2 screws		**ZORAN**	Drawing available

Notes

Unless otherwise specified:

1. ALL resistors are 0.125 watt, 5% tolerance, SMT: 0805 or 1206 package.
2. ALL capacitors are ceramic, 50 volt, 20% max. tolerance, SMT: 0805 or 1206 package.
3. ALL 74XXX chips are SMD-SOIC package type.
4. ALL components are standard, not custom manufactured. Components that are from a specific manufacturer are **BOLD** (In the Manufacturer column).
5. Through hole resistors are 0.125 watt, 5% tolerance.
6. Through hole capacitors are ceramic, 50 volt, 20% max. tolerance.
7. Tantalum SMD capacitor package size codes (SMD-XX) are taken from the 1988 Mallory capacitor catalog. Unless otherwise specified all tantalum SMD capacitors are 16 volt.

Abbreviations:

Cap. - Capacitor
Res. - Resistor
TH - Through Hole / PCB
90-TH = 90 degrees TH / PCB
Tan. - Tantalum Cap.
Elc. - Electrolytic Cap.
Cer. - Ceramic Cap.
NC - Not Connected / Not Stuffed
Conn.- connector
Osc. - oscillator

Assembly Comments :

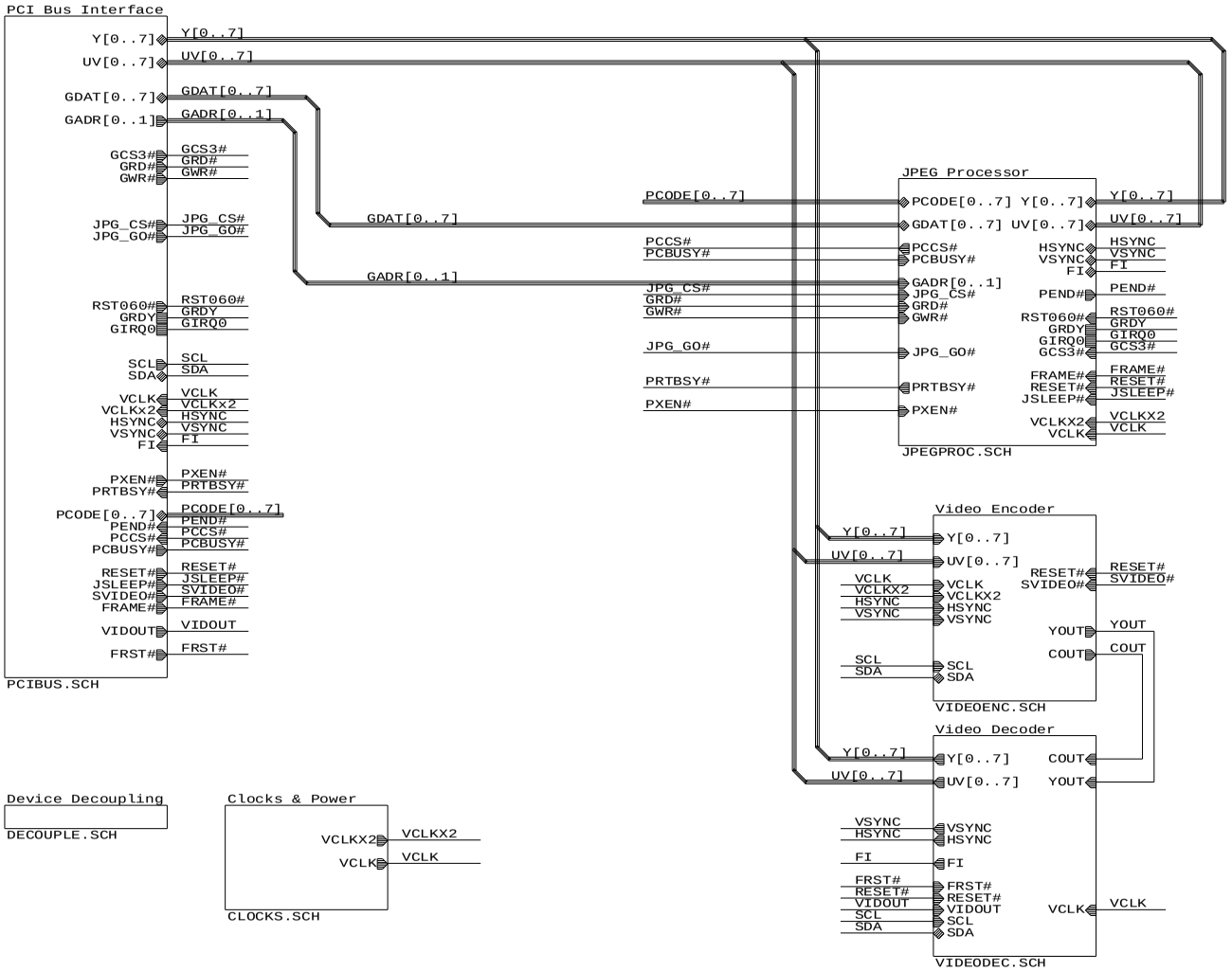
1. Assembly comments are **BOLD** in the Comments column.

Appendix C

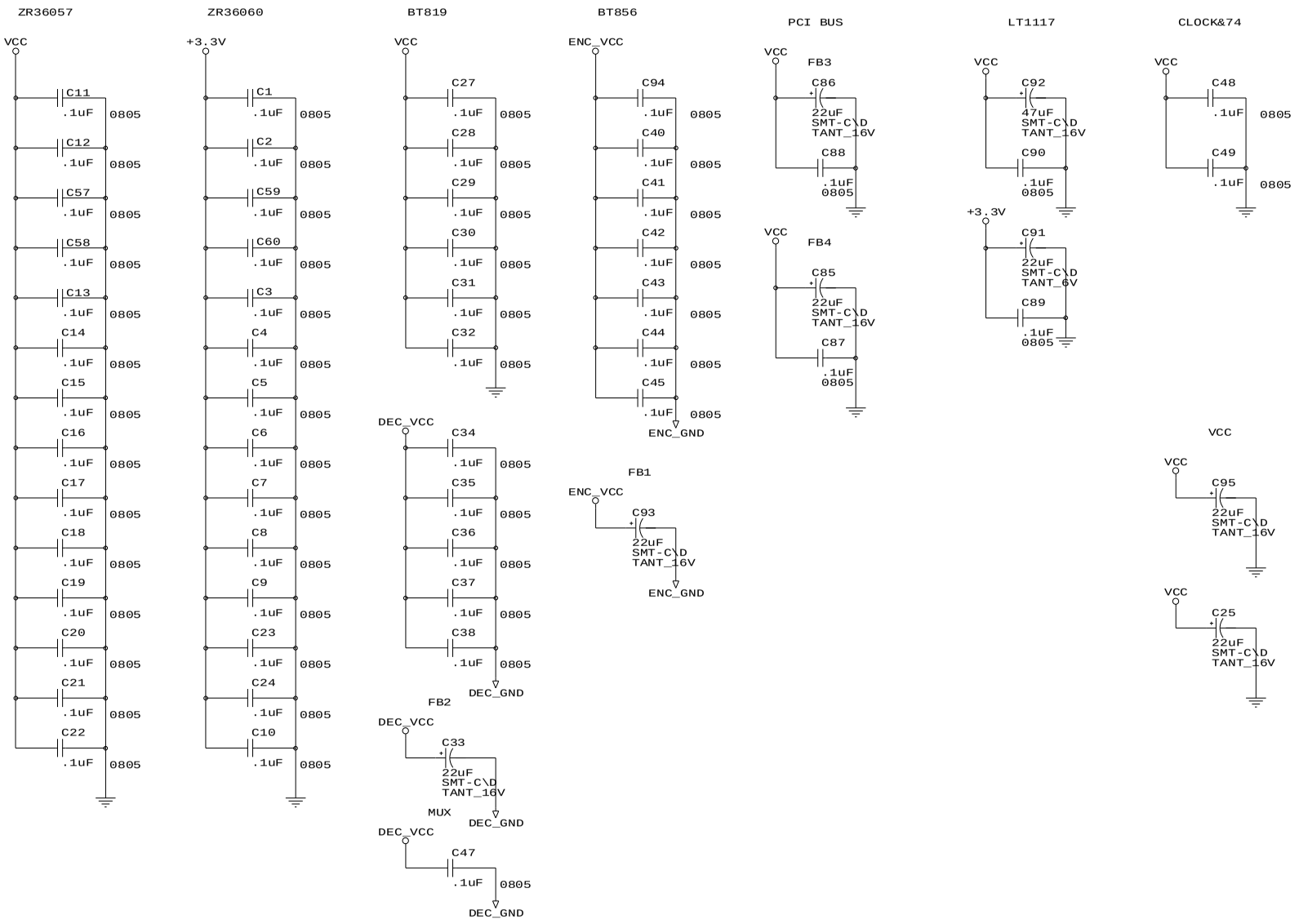
Schematics (next 7 pages)

SCHEMATICS ARE SUBJECT TO CHANGE WITHOUT NOTICE

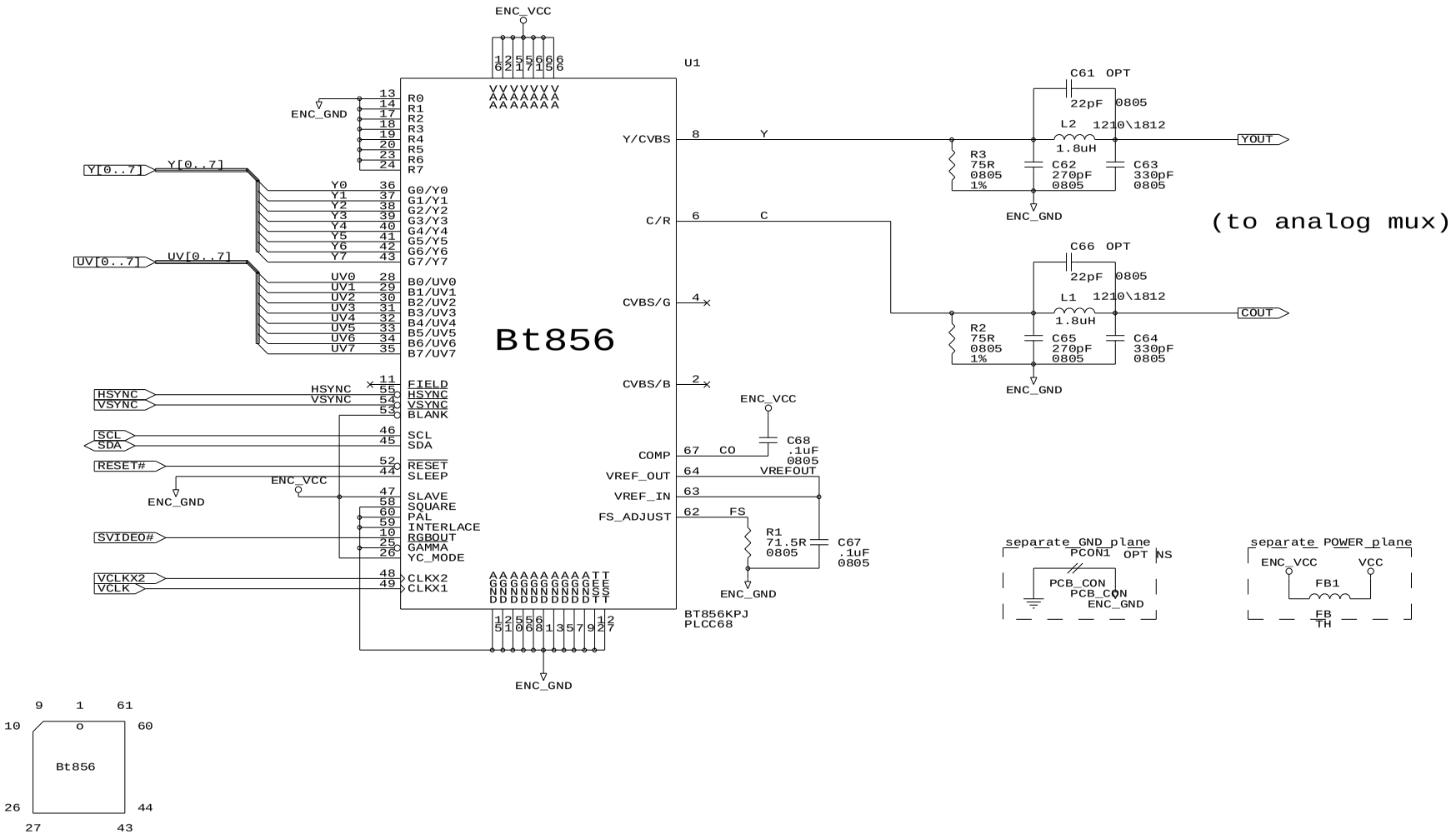
ZR36060 Reference Design Board (H33R)



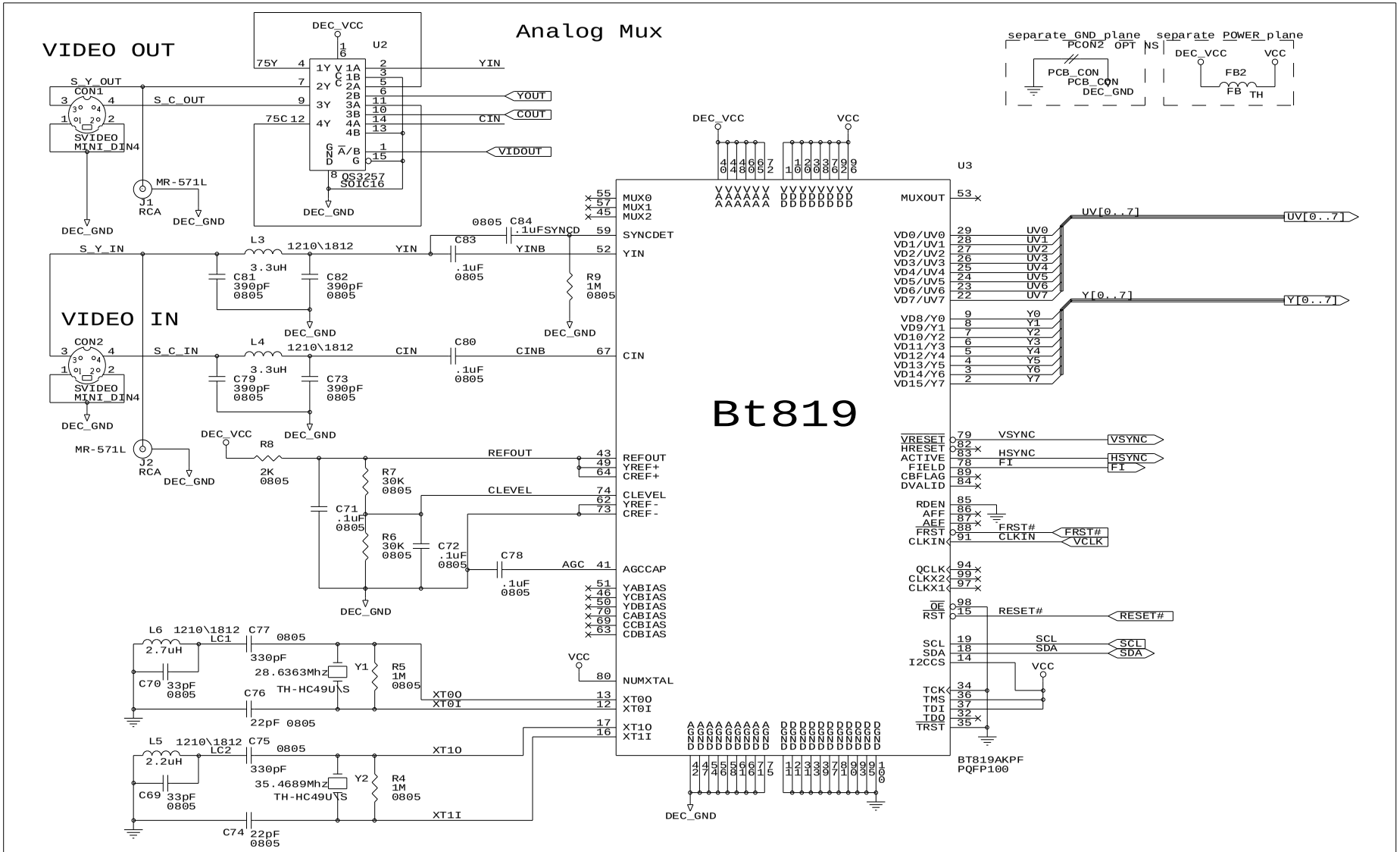
ZORAN Corporation	
System Engineering Group	
PROPRIETARY INFORMATION	
Title	ZR36060 Reference Design (H33R)
Size: B	Document Number: H33R.SCH
REV: 1.0	
Date: May 9, 1997	Sheet 1 of 7



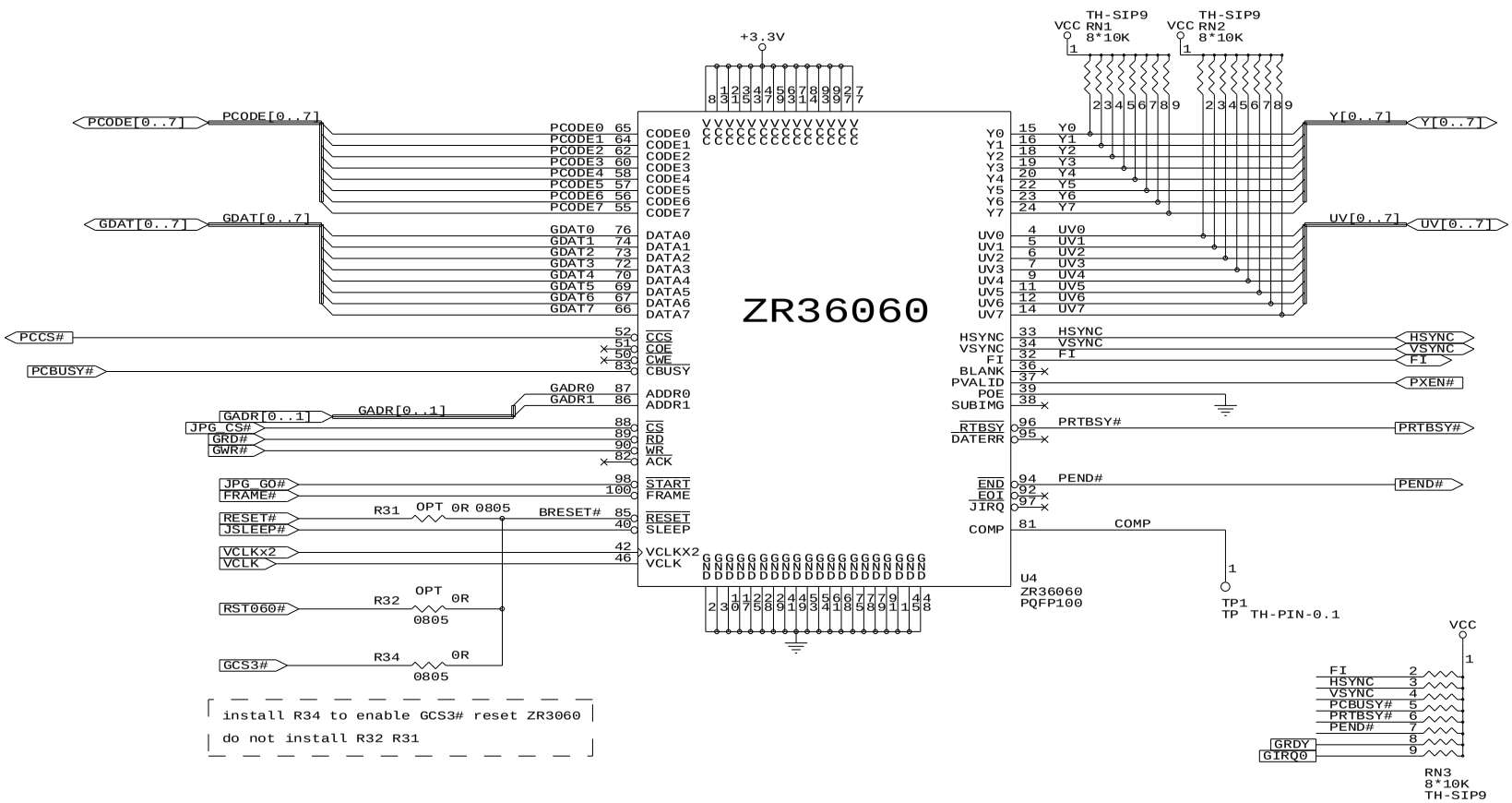
ZORAN Corporation		
System Engineering Group PROPRIETARY INFORMATION		
Title: H33R Decoupling Caps		
Size: B	Document Number: DECOUPLE.SCH	REV: 1.0
Date: May 9, 1997	Sheet 2 of 7	



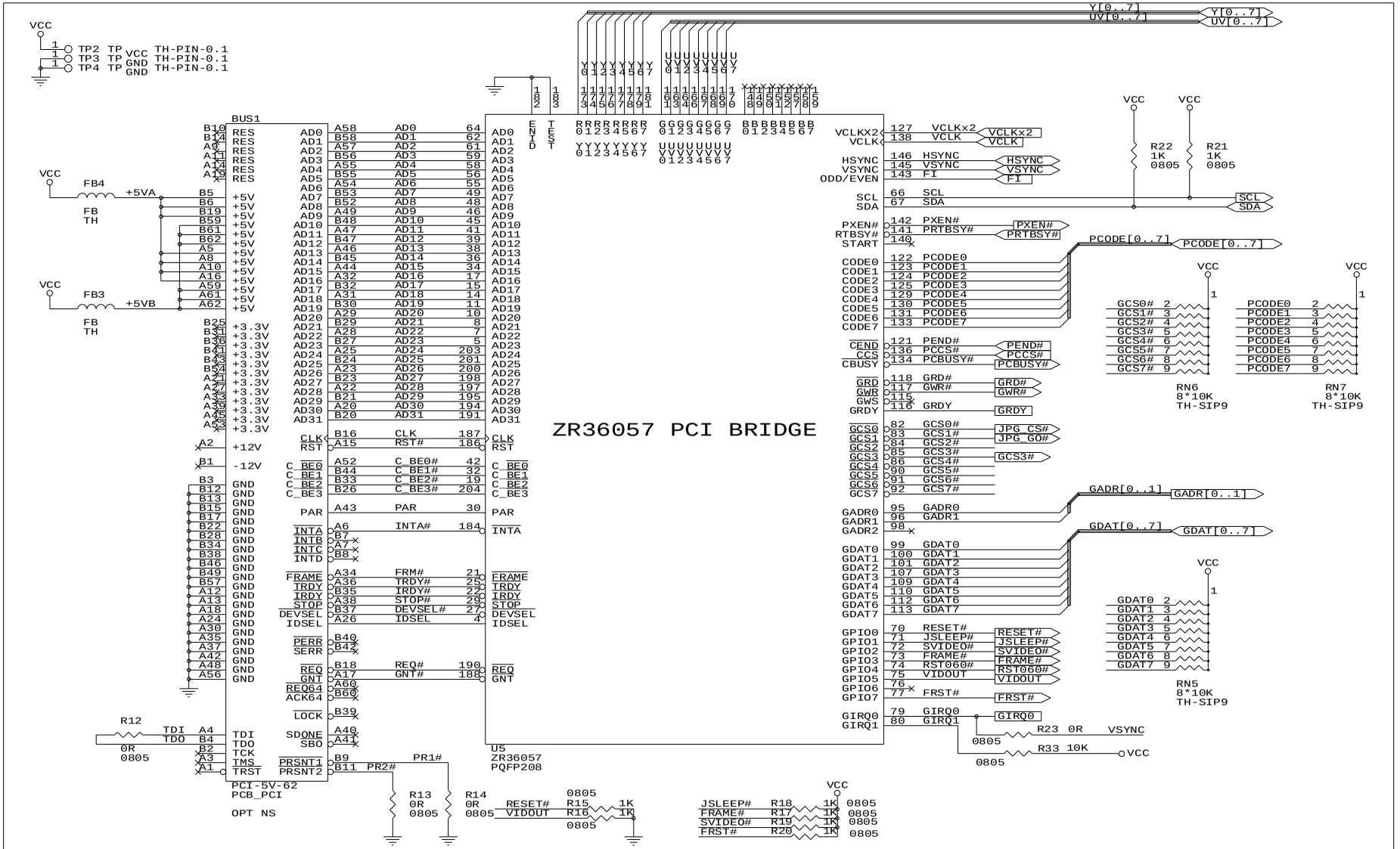
ZORAN Corporation		
System Engineering Group PROPRIETARY INFORMATION		
Title: H33R Video Encoder		
Size: B	Document Number: VIDEOENC.SCH	REV: 1.0
Date: May 9, 1997	Sheet 3 of 7	

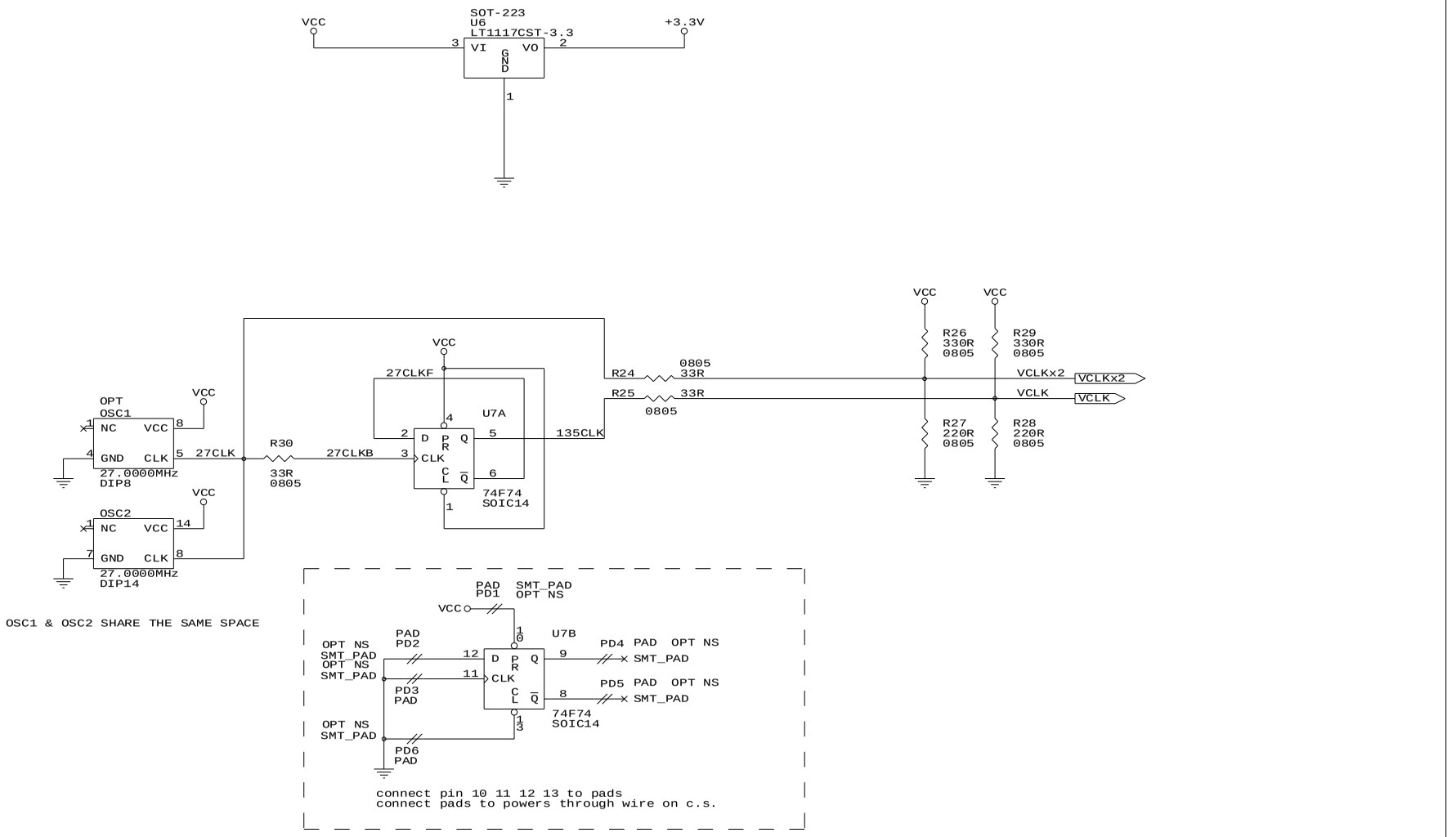


ZORAN Corporation System Engineering Group PROPRIETARY INFORMATION		
Title: H33R Video Decoder		
Size: B	Document Number: VIDEODEC.SCH	REV: 1.0
Date: May 9, 1997	Sheet 4 of 7	



ZORAN Corporation System Engineering Group PROPRIETARY INFORMATION		
Title: H33R JPEG Processor		
Size: B	Document Number: JPEGPROC.SCH	REV: 1.0
Date: May 9, 1997	Sheet 5 of 7	


ZR36057 PCI BRIDGE
U5
ZR36057
PQFP208
BUS1
PCI-5V-62
PCB_PCI
OPT NS
TP2 TP VCC TH-PIN-0.1
TP3 TP GND TH-PIN-0.1
TP4 TP GND TH-PIN-0.1
FB4 +5VA
FB3 +5VB
FB TH
Y[0..7]
UV[0..7]
VCLKx2
VCLK
HSYNC
VSYNC
FI
SCL
SDA
PXEN#
PRTBSY#
START
PCODE[0..7]
CEND
CCS
CBUSY
GRD
GWR
GWS
GRDY
GCS0
GCS1
GCS2
GCS3
GCS4
GCS5
GCS6
GCS7
GADR[0..1]
GADR0
GADR1
GADR2
GDAT[0..7]
GDAT0
GDAT1
GDAT2
GDAT3
GDAT4
GDAT5
GDAT6
GDAT7
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GIRQ0
GIRQ1
RESET#
JSLEEP#
SVIDEO#
FRAME#
RST060#
VIDOUT
FRST#
JPG_CS#
JPG_GO#
GCS3#
PEND#
PCCS#
PCBUSY#
GRD#
GWR#
GRDY
R12 TDI TDO 0R 0805
R13 0R 0805
R14 0R 0805
R15 1K 0805
R16 1K 0805
R17 1K 0805
R18 1K 0805
R19 1K 0805
R20 1K 0805
R21 1K 0805
R22 1K 0805
R23 0R 0805
R33 10K 0805
RN5 8*10K TH-SIP9
RN6 8*10K TH-SIP9
RN7 8*10K TH-SIP9
VCC
ZORAN Corporation
System Engineering Group
PROPRIETARY INFORMATION
Title
H33R PCI Bus Interface
Size B
Document Number PCIBUS.SCH
REV 1.0
Date: May 9, 1997 Sheet 6 of 7



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Title H33R Clocks & 3.3V Power		
Size B	Document Number CLOCKS.SCH	REV 1.0
Date: May 9, 1997	Sheet 7 of 7	