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# AMD Geode™ LX EPIC SBC RDK Hardware Developer's Guide



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## 1.0 Scope

The AMD Geode™ LX processor embedded platform for industrial computing (EPIC) single board computer (SBC) reference design kit (RDK) (hereafter referred to as LX EPIC RDK) provides a complete system solution, including schematics, layout, bill of materials (BOM), and documentation. The intent of this document is to describe the overall hardware design of the board, provide insight on key design constraints, and where appropriate, provide design alternatives.

## 2.0 Overview

The AMD Geode™ LX EPIC RDK is implemented in the EPIC PC/104-Plus compatible form factor, which provides support for the AMD Geode™ CS5536 companion device. Full ISA compatibility is provided through a PCI-to-ISA bridge.

Building on AMD's philosophy of delivering low total cost of ownership, the LX EPIC RDK is optimized to provide value through all phases of the design and development cycle (device choices, schematics, layout, and software). It was designed to provide an extensible solution for both hardware and software, while serving as a powerful, manufacture-ready reference design tool.

It is intended to provide a complete solution for both hardware and software, or can be used as a powerful beginning for a differentiated design. As a complete solution, utilizing the AMD Geode solutions design flexibility, the LX EPIC RDK helps reduce the costly time-to-market concerns; while at the same time creating an effective, efficient embedded computer design.

The LX EPIC RDK is based on proven, third generation AMD Geode RDK technology, providing a complete system design package that gives designers flexibility, versatility and enhanced capabilities. The LX processor provides the flexibility of the x86 instruction set with the power to run current popular operating systems.

The LX EPIC RDK and other advanced development tools represent AMD's commitment to low-power customer-centric solutions for the x86 embedded marketplace by providing an integrated suite of support and development capabilities. The LX EPIC RDK contains materials needed to quickly and efficiently move embedded computing solutions to market.

## 2.1 Application Markets

The LX EPIC RDK features a flexible design that can address a broad range of embedded devices such as:

- Single Board Computer
- Corporate Thin Client
- Network Devices
- Point-of-Sale (POS)
- Education
- Kiosk

## 3.0 Board Devices

This section describes the hardware devices found on the board.

### 3.1 Processor

The AMD Geode™ LX processor provides the foundation of the design. This component integrates the CPU core, memory controller, and graphics subsystem from traditional designs into a single chip, reducing system cost and complexity.

#### 3.1.1 Package Type

The LX EPIC RDK is built using the LX processor in the BGU481 (481-Terminal Ball Grid Array Cavity Up) package. The BGU481 package contains an internal heat spreader to aid in CPU cooling.

#### 3.1.2 CPU Core

The x86 core of the LX processor is transparent in the hardware design of the system. The LX EPIC RDK is built with a 500 MHz CPU core speed by default, though the design also supports a 433 MHz CPU core.

#### 3.1.3 Memory Controller

The LX processor provides an integrated DDR SDRAM memory controller with a 64-bit wide access path. A single SODIMM is connected directly to the LX processor without parallel termination resistors, thus providing a lower part count and simplified routing. For more detailed information, refer to Section 3.3 on page 4.

### 3.1.4 Graphics Subsystem

The AMD Geode LX processor includes an integrated 2D graphics accelerator, display controller, digital TFT interface and CRT DACs. The display controller is capable of in-hardware color conversion and palletized color. In addition, the LX processor contains proprietary compression hardware that reduces the overall load on the memory bus.

The LX processor utilizes system DDR SDRAM within the unified memory architecture (UMA) to store the graphics/video frame buffer. The frame buffer may be up to 16 MB in size, but may be reduced to 8 MB for systems using 1280x1024x16 or smaller graphics resolutions. For the lowest graphics resolutions, 4 MB is sufficient. For the highest graphics resolutions or graphics-intensive applications, 16 MB frame buffer sizes are recommended, though this reduces the overall available system RAM.

The system supports graphics modes of 16 and 24 bpp and resolutions from 640x480 to 1600x1200. A 320x240 graphics resolution is also supported for TFT displays.

#### 3.1.4.1 Graphics Subsystem Output

Both analog CRT and digital TFT outputs are supported. The LX EPIC RDK supports simultaneous video output to both TFT and VGA display with both displays rendering identical data at an identical resolution.

CRT output is wired to a VESA compliant HD15 connector. TFT output is wired to a 30-pin Hirose connector (J2). Additionally, the TFT interface is converted to a Low Voltage Differential Signaling (LVDS) interface wired to a 20-pin Hirose connector (J28). The TFT interface provides a switched 3.3V power source supplying up to 1A for TFT electronics. The RDK provides an additional header (J30) to supply a 12V power source and pulse-width-modulated brightness control signal to the TFT backlight inverter. This power source must come from 12V rails, as 5V is not sufficient.

#### 3.1.5 High-Speed Data Port

The LX processor contains a 16-bit high-speed data input port (HSDIP), which provides a direct data interface to an internal DMA engine. The HSDIP supports message passing and data streaming modes at a maximum data rate of 150 MHz. The HSDIP is wired to a 40-pin stake pin connector (J3) on the LX EPIC RDK.

## 3.2 Companion Device

The LX EPIC RDK supports the AMD Geode™ CS5536 companion device for system peripheral connectivity.

### 3.2.1 GPIO Usage

The CS5536 companion device provides up to 28 GPIOs, with most having alternate functions. BIOS and bootloaders developed for this RDK generally expect certain functionality to be selected on the GPIOs. It is strongly recommended that system developers do not arbitrarily change the usage model of the GPIOs in the RDK as this will impact BIOS and/or bootloader development. Care must be taken when adding features, as a GPIO/feature conflict may occur. Four GPIOs are wired to an internal 40-pin stake pin header (J13): GPIO6, GPIO8, GPIO9, and GPIO25. The header also provides 3.3V, 5V, and 3.3 VSB (Standby) voltages. If additional GPIOs are required, the SuperI/O (SIO) device (see Section 3.6 on page 4) on the LX EPIC RDK may be used to provide additional GPIO signals.

### 3.2.2 MFGPT

The CS5536 companion device provides eight Multi-Function General Purpose Timers (MFGPTs). Six of these timers operate in the Working power domain, and may use 32 KHz or 14.318 MHz clock sources. Two of these timers operate in the Standby power domain, and use a 32 KHz clock source only. GPIO6 and GPIO25, which are wired to an internal 40-pin stake pin header (J13), alternately support some MFGPT functionality. GPIO6 is connected to the Working power domain and GPIO25 is connected to the Standby power domain.

### 3.2.3 Boot Options

Booting from the Low Pin Count (LPC) or Flash (IDE) ports is selected via a strap option. If a pull-down resistor is connected to the AC\_S\_OUT/BOS1 signal (ball L2 of the CS5536), the system boots from the LPC port. If a pull-up resistor is connected to the signal, the system boots from NOR Flash on the IDE port. By default, the LX EPIC RDK is configured to boot from the LPC port, but the system may be configured either way.

#### 3.2.3.1 Bootstrap Options

Three boot options for the CS5536 companion device are available:

BOS1 (Ball L2)	BOS0 (Ball L3)	Description
L	L	LPC ROM off LPC
H	L	NOR FLASH off IDE
L	H	Reserved
H	H	SST FWH off LPC (default)

### 3.2.4 LPC Bus

The Low Pin Count (LPC) bus is an industry standard interface utilized for connecting to legacy device interfaces. The LX EPIC RDK uses the LPC bus to interface with an ITE IT8712 SIO device to provide legacy connectivity. This device is discussed in greater detail in Section 3.6 on page 4.

In addition, the LX EPIC RDK provides a LPC header (J8) to allow an external LPC device, such as LPC Flash ROM, to be added to the system.

### 3.2.5 IDE and Flash Interface

The CS5536 companion device provides a pin-multiplexed interface that may be configured as either a standard IDE interface or a Flash memory interface. The Flash interface allows for direct connection to a NAND Flash device or, with proper latching, connection to a parallel address/data interface. The IDE port supports ATA standard devices, such as DiskOnModule or a hard disk drive, for mass storage.

DiskOnModule is a standard that uses an IDE controller front end connected to NAND Flash device(s). It can plug directly into a 44-pin IDE header. The system must be configured to boot from LPC using a DiskOnModule.

The LX EPIC RDK provides a 44-pin 2 mm IDE header (JHDD1) for the attachment of mass storage or alternative boot devices. The interface supports up to two UDMA100 capable devices. Alternatively, this interface may be used to connect NAND or NOR Flash devices as supported by the CS5536 companion device.

By default, the 44-pin IDE header supplies 5V at up to 1A to pin 42. This pin may be configured to supply 3.3V at up to 250 mA through resistor loading options.

#### 3.2.5.1 IDE Design Considerations

- The IDE interface is 5V tolerant.
- 80-wire cable detection components: 10K and 47 nF in parallel tied to GND on pin 34 of connector.
- 10K pull-down is required on D7 to prevent system BIOS from thinking that a drive is connected and busy during IDE auto-detect routines.
- Dynamic switching of port between IDE and Flash port not supported. Flash port may be used for system initialization, then switch to IDE, though additional circuitry is required to support DMA under this circumstance.

### 3.2.6 USB

The CS5536 companion device provides a total of four USB v2.0 compliant host ports. These ports are brought out to four external USB type-A connectors (stacked with RJ-45 Ethernet connectors) on the LX EPIC RDK. USB port 4 (J15, top port) may be configured to act as a USB v2.0 compliant device port. The system design utilizes a resettable fuse to limit the current to the ports.

In addition, USB port 3 (J15, bottom port) is brought out to an internal  $\mu$ DOC-compatible header (J16). If the  $\mu$ DOC device is present, the external type-A connector is disabled. If the  $\mu$ DOC device is not present, the  $\mu$ DOC header must have jumpers installed to pass USB connectivity to the type-A connector.

### 3.2.7 RTC and CMOS

The system uses a 3V BR2032 Li-ion coin-cell battery to supply power to the Real-Time Clock (RTC) circuit inside the CS5536 companion device. This battery has a 190 mAh capacity. The CS5536 companion device's input current from the battery is 5  $\mu$ A maximum (typical is 2  $\mu$ A at 25°C) Therefore, the battery should last at least 38,000 "system off" hours as a worst-case scenario. Typical battery life is much longer.

### 3.2.8 SMB Interface

The CS5536 companion device provides a System Management Bus (SMB) interface for serial communication with and configuration of devices. The SMB interface also supports the industry standard 2-wire interface and ACCESS.bus specifications. The interface is capable of operating in master or slave mode.

SMB is an open-collector interface, and both clock and data lines must be attached to 2.2K or 10K pull-up resistors.

### 3.2.9 AC97 Interface

The CS5536 companion device provides an AC97 specification v2.3 compliant interface for communication with modems and audio codecs. The LX EPIC RDK utilizes this interface to operate a Realtek ALC655 audio codec device. For more detailed information, refer to Section Section 3.8 on page 5.

### 3.3 Memory Interface

The LX EPIC RDK utilizes a single standard SODIMM socket connected directly to the LX processor memory controller. The RDK supports SODIMM modules containing up to eight memory devices. The use of an SODIMM socket provides system flexibility, and allows the system to operate without the  $V_{TT}$  termination rail prescribed for JEDEC standard DDR SDRAM without compromising signal integrity. Removal of this voltage rail reduces both system cost and power consumption significantly.

The LX EPIC RDK supports memory devices up to DDR400 memory timings. Latencies are configurable over the full range allowed in the JEDEC standards. This allows CAS latency down to 1.5 clocks.

A Serial Presence Detect (SPD) ROM device is usually implemented on the memory module, allowing the memory controller to be properly configured (memory configuration, size, and timings) by the BIOS or bootloader. If a custom design requires the lowest cost and highest integration, discrete SDRAM devices can be soldered on-board, with their configurations hard-coded into BIOS.

### 3.4 JTAG Interface

The JTAG debug interface is connected in a daisy chain mode between the LX processor and CS5536 companion device. Additional JTAG-capable devices added to the design may be added to the daisy chain.

### 3.5 PCI Interface

The LX processor and CS5536 companion device are compliant with PCI specification v2.2. The LX EPIC RDK PCI bus provides connectivity to the following devices and headers:

- PCI-104 stackable connector (four PCI "slots")
- ITE IT8888 PCI-ISA bridge (for PC/104 stackable connector)
- Micrel RTL8100 Ethernet controller
- Mini PCI connector

Including the CS5536 companion device, the system contains a total of eight devices that require REQ/GNT pairs. The system incorporates two 1-to-3 PCI expanders, creating a total of seven available pairs. The Ethernet controller, Mini PCI connector, and PCI-104 slot 4 share two of these pairs, therefore only two of the three devices may be active at a time. The active devices are selected using jumpers.

#### 3.5.1 PCI-ISA Bridge

The EPIC specification requires ISA bus support to be in compliance with the PC/104-Plus specification. The LX EPIC RDK utilizes an ITE IT8888 PCI-to-ISA bridge device to provide this support. The IT8888 supports distributed DMA, which is the only ISA DMA solution supported in a LX processor/CS5536 companion device system.

### 3.6 Super I/O

The LX EPIC RDK incorporates the ITC IT8712 SIO device over the LPC bus to provide legacy connectivity support.

#### 3.6.1 SPI Interface (BIOS Flash)

The LX EPIC RDK uses a 512 KB SPI (Serial Peripheral Interface) Flash ROM as the default boot Flash device. This device is connected to the IT8712, which is in turn selected as the boot device (over the LPC bus) by the BOS[0:1] resistor loading option to the CS5536 companion device.

#### 3.6.2 UART

The ITC IT8712 provides support for two 16C550 enhanced UART serial ports. Both serial ports support full modem/flow control signals. On the LX EPIC RDK, both serial ports are connected through RS232/RS485 transceivers; port 1 to an external DB-9 connector, and port 2 to an internal 10-pin stake pin header (J19). SIO\_GPIO11 and SIO\_GPIO12 are used to select the transceiver mode.

#### 3.6.3 Floppy Disk Controller

The ITC IT8712 provides the floppy disk controller for the LX EPIC RDK. The IT8712 supports up to two 360K, 720K, 1.2M, 1.44M, or 2.88M floppy drives. The floppy drive controller is brought out to an external 26-pin ribbon cable connector (J20) that is compatible with laptop floppy drives.

#### 3.6.4 Parallel Port

The ITC IT8712 provides a IEEE1284 compliant parallel interface. This interface supports Extended Capabilities Port (ECP), Enhanced Parallel Port (EPP), and Standard Parallel Port (SPP) modes. On the LX EPIC RDK, this interface is brought out to an external DB-25 port.

#### 3.6.5 PS/2 Interface

The ITC IT8712 provides two 8042 compatible ports for PS/2 keyboard and mouse support. On the LX EPIC RDK, these ports are brought out to two stacked external PS/2 headers.

### 3.6.6 PWM and ADC

The ITC IT8712 provides five Pulse-Width Modulation (PWM) signals for fan speed control, each variable by 128 steps. On the LX EPIC RDK, one of these signals is allocated for fan speed control, while the remaining four signals are routed to an internal stake pin header (J12) for use as general purpose PWM outputs.

The IT8712 also provides an 8-channel, 8-bit Analog-to-Digital Converter (ADC) for thermal, battery, and voltage monitoring. The ADC has a 16 mV LSB, with a 0V to 4.096V input range. Higher voltage inputs must be divided into the acceptable range with recommended resistor values for the divider circuit ranging from 10K to 100K. The conversion rate is 8 Hz maximum. Use of the ADC is limited to applications that can accept this frequency. In the LX EPIC RDK system, all eight ADC inputs are routed to an internal stake pin header (J12) for general use.

### 3.6.7 GPIO

The ITC IT8712 provides an additional 48 GPIO signals to the system. These signals share pins with other components of the IT8712, so a specific GPIO signal's availability may change depending on the function set with which the IT8712 is configured. The IT8712's GPIO signals incorporate special functionality for various system needs, including watchdog timer, external interrupt routing, SMI# output routing, button de-bounce, keyboard lock input routing, LED blinking, thermal output routing, and beep output routing.

On the LX EPIC RDK, 26 of the IT8712's GPIO signals have been routed to an internal stake pin header (J13) for general use. Other GPIO pins are used by the system for their alternate pin functionality. It is strongly recommended that system developers do not arbitrarily change the usage model of GPIOs other than the 26 allocated for general use in the RDK, as this may impact BIOS and/or bootloader development.

## 3.7 Ethernet Controller

The Micrel KSZ8842 is a highly-integrated, single-chip, dual-PHY fast Ethernet controller with a 32-bit performance, 33 MHz PCI interface with bus master capability. The KSZ8842 is fully compliant with IEEE 802.3u 100Base-T specifications, and IEEE 802.3x full-duplex flow control. The controller also supports PCI-based power management and Wake-on-LAN functionality. The KSZ8842 includes serial EEPROM support for non-volatile storage of configuration information including MAC address and ID.

On the LX EPIC RDK, the two Ethernet PHYs of the KSZ8842 are connected to two external RJ-45 Ethernet connectors (stacked with USB connectors) with integrated indicator LEDs. Note that the KSZ8842 may not be enabled

on the PCI bus depending on system settings (see Section 3.5 on page 4).

Other Ethernet controllers may be selected for use in a custom solution. Software drivers are generally provided by the vendor, removing the need for extra software development. Additional or alternate system requirements may require different solutions. Gigabit Ethernet, 66 MHz PCI, security requirements, or low-power considerations may cause a different device to become the optimal selection. Micrel and other vendors provide many different Ethernet solutions.

## 3.8 Audio Codec

The Realtek ALC655 is a 16-bit, full duplex AC97 v2.3 compliant 6-channel audio codec. The codec is connected to the CS5536 companion device via the AC97 interface. The ALC655 provides three pairs of stereo outputs with 5-bit volume controls, a mono output, and multiple stereo and mono inputs, along with flexible mixing, gain, and mute functions.

The codec incorporates impedance-sensing technology to detect device load on outputs and inputs. The ALC655 also supports multiple codec extensions, with multiple sampling rates and built-in 3D effects. The codec further provides a power-off CD function, which passes the analog CD-IN signal through the output amplifier, allowing audio playback while the system is shut down. The 3.3V digital power must be off in this state, and 5V analog power must be supplied to the codec.

The digital interface to the ALC655 operates from a 3.3V power supply, while the analog components may operate from 3.3V or 5V power sources. Both of these supplies are readily available in the LX EPIC RDK system. The codec integrates 50 mW/20 $\Omega$  headset audio amplifiers at Front-Out and Surr-Out, a 14.318M24.576 MHz PLL, and a PCBEEP generator, removing the need for these external components and reducing BOM cost.

### 3.8.1 6-Channel Surround

The Realtek ALC655 provides dedicated outputs for 6-channel surround sound (Front L/R, Surround L/R, and Center/LFE). However, the LX EPIC RDK uses the muxed input/output feature of the codec to reduce the required number of external jacks. With this configuration, the Line-In jack is shared with Surround-Out, and the Microphone-In jack is shared with Center/LFE-Out. These jacks are connected to the impedance-sensing inputs of the codec to enable software to determine which jack configuration to use. A system requiring dedicated input and output ports may connect additional external jacks to the dedicated outputs of the ALC655.

### 3.8.2 Microphone

The system provides an internally-biased microphone jack. Only a passive microphone should be connected to this jack. A passive microphone does not require a separate power source, whereas a biased microphone requires its own bias voltage supply. The ALC655 provides a 20 dB analog boost on the microphone input.

### 3.8.3 Alternate Codec Options

The CS5536 companion device provides a fully AC97 v2.3 compliant audio link, therefore other codec devices, including those from other vendors, may be used to provide a custom audio solution. However, as codecs may vary in their configuration and programming, the selection of a different codec device may result in custom driver work to support vendor- and device-specific features. Some audio codecs incorporate non-audio functionality, such as touch-screen inputs, which may provide a low-cost solution for a custom system with these requirements.

### 3.8.4 Audio Design Considerations

The system must provide a separate ground plane for the analog audio components of the system and audio codec. Digital ground should tie into this plane at a single point. This should be a wire connection, not a ferrite connection.

## 3.9 Clocking

The ICS MK1491-09 is a low cost, low jitter, high performance clock synthesizer for the LX processor. Using patented Phase-Locked Loop (PLL) techniques, the device accepts a 14.318 MHz crystal input to produce multiple output clocks. The MK1491-09 provides selectable PCI local bus clocks, 48 MHz clocks for SIO, and multiple reference outputs. Low EMI Enable reduces electromagnetic interference (EMI) on PCI clocks, LCLKs, and the 66 MHz clock by producing a spread spectrum clock. The device also provides a power-down mode to reduce power consumption.

While other clock generators may be used, the MK1491-09 is highly recommended as it is specifically designed for use with the LX processor and CS5536 companion device.

### 3.9.1 Companion Device

The CS5536 companion device requires a 32 KHz clock for proper operation: KHZ32\_XCI (ball A4) and KHZ32\_XCO (ball B3). For the XTAL circuit, a 20M resistor is required. Two 10M in series may be used in case of availability or BOM-reduction concerns. If driven by an oscillator, the output signal must not be present when there is no  $V_{BAT}$  or  $V_{IO\_USB}$ , or ESD protection diodes could be damaged. KHZ32\_XCO must be no-connect (NC) if an oscillator is used. There is also an on-chip 48 MHz oscillator and an external crystal to supply the low jitter clocking requirements of USB.

### 3.9.2 DRAM Clocks

Unused DRAM clocks will be toggling, and should not have traces in order to reduce EMI.

## 3.10 PC/104-Plus Connectors

The EPIC specification is designed to be fully compatible with PC/104, PCI-104, and PC/104-Plus stackable modules. The PC/104 specification provides a 104-pin ISA header for both 8-bit and 16-bit ISA modules. The PCI-104 specification provides a 120-pin PCI header for 32-bit PCI modules. The PC/104-Plus specification provides both headers for maximum bus flexibility.

The LX EPIC RDK provides both the 104-pin ISA header (J21A and J21B) as well as the 120-pin PCI header (J22A and J22B) as defined by the PC/104-Plus specification. In addition, the RDK provides "stack-through" headers, allowing the modules to be attached from both sides of the baseboard. Although the RDK may be physically attached on top of another EPIC baseboard, it is not capable of acting as a PCI or ISA slave.

The 120-pin PCI header is designed to accommodate four REQ/GNT pairs, effectively providing four PCI "slots." As discussed in Section 3.5 on page 4, the fourth REQ/GNT pair on the RDK is shared with the mini-PCI slot and Ethernet controller. Only two of these devices may be active at once, therefore the fourth PCI-104 slot may be disabled in favor of these two devices.

## 4.0 Power

The LX EPIC RDK supports the following ACPI power states:

- S0/C0 – Working
- S0/C1 – Halt
- S1 – Power-On Suspend
- S3 – Suspend-to-RAM
- S5 – Soft Off

### 4.1 External Power Supply

The LX EPIC RDK is powered by a Mini-ATX power supply connected to a 10-pin Mini-ATX connector (J25). The power supply provides +12V, +5V, +5V Standby, +3.3V, and -12V. The EPIC RDK board devices use only +5V and +5V Standby. +5V is also used to supply the IDE and floppy interfaces. +12V or +5V can be used to supply the LCD backlight converter. +12V, +5, +3.3V and -12V supply the PC/104-Plus plug-in cards.

A simple configuration was tested to measure the power consumption of the LX EPIC RDK board. The configuration was as follows:

- LX EPIC RDK board
- 2.5 inch hard drive
- PS2 keyboard
- PS2 mouse
- Monitor

The PC99 benchmark was used as the test application. +5V/+5V Standby average and maximum power was measured at the input of the board yielding the following results:

Voltage	Average	Maximum
+5V	6W	9.5W
+5VSB	1.1W	2W

## 4.2 Internal Voltages

In addition to the voltages provided by the Mini-ATX power supply, five internal voltage rails are created from the external +5V and +5V Standby supplies: 3.3V, 3.3V Standby, 2.6V, 1.25V, and 1.225V. The 1.25V rail exists in the Working domain and powers the LX processor core, while the 1.225V rail exists in the Standby domain, and powers the LX processor core when in Standby mode. The 2.6V rail exists in the Standby domain, and powers the DDR SDRAM interface. The 3.3V rails power most of the remaining system devices.

## 4.3 Power Switches and LED

The power and reset switches (SW1 and SW2, respectively) are located near the Mini-ATX power supply connector at the back of the LX EPIC RDK. Pressing the power switch while the system is off (S5) causes the system to power on. Pressing the power switch while the system is on (S0) causes the system to enter Standby mode (S1 or S3, depending on BIOS settings). Holding the power switch for four seconds while the system is on (S0) causes the system to power off (S5). Pressing the reset switch at any time the system is not powered off (S5) reboots the system with an immediate soft-reset.

An optional green LED (D14) indicates the system is powered and running. The LED is off when the system is in Standby mode. An optional red LED (D2) may be used to indicate a low backup battery voltage.

## 4.4 Power Considerations

- The 3.3V Standby supply to the CS5536 VIO\_VSB pin must be able to supply 5 mA.
- Required power sequence: 5V Standby/3.3V Standby -> 1.225V/5V/3.3V -> 2.6V -> 1.25V
- The CS5536 companion device internal battery circuit is currently pending UL approval. Once UL approval is granted, the 47 $\Omega$  protection resistor (R1) may be removed from the design.
- Power button requires a minimum button push time of 64  $\mu$ s, with a maximum rise time of 60 ns.

## 5.0 Debug

While the LX EPIC RDK is designed to be a complete solution, some debug support is provided. Three levels of debug tools are available which have tradeoffs between features and cost.

### 5.1 FS2

The LX processor design team worked with First Silicon Solutions (FS2) (<http://www.fs2.com/geodetools.html>) to create a very high featured JTAG debugger called the System Navigator.

FS2 and AMD jointly developed special silicon hooks for software debug and system testing, which are integrated into the processor. These On-Chip Instrumentation (OCI) extensions allow FS2 to provide a powerful debug tool with advanced features at a competitive price. The System Navigator is used for hardware testing and integration, BIOS development, and other firmware/software testing. In addition to hardware and software breakpoints, processor run control, and access to all the CPU registers and coprocessor registers, the FS2 System Navigator has on-chip and off-chip trace features. Trace information is decoded and displayed as executed instructions. Traces can either be captured in on-chip memory (128 64-bit frames) or streamed off-chip (64K 64-bit frames) for collection in the FS2 probe. The trace window displays disassembled instructions interspersed with special messages such as interrupts and exceptions.

The System Navigator is contained in a compact chassis that connects to the LX EPIC RDK using a 14-pin JTAG connector (J7). The optional off-chip trace connector is not provided on the RDK, therefore only on-chip trace functionality is usable on this design. The system runs on a PC with a Windows<sup>®</sup> 98, Windows NT, Windows 2000, or Windows XP operating system over an IEEE-1284 EPP/ECP high-speed parallel port or USB port. A graphical source debugger program provides the user with an intuitive, easy to use interface.

### 5.1.1 Key Features

- Utilizes On-Chip Instrumentation (OCI) debug extensions in the LX processor
- Read/write all CPU registers, Model Specific Registers (MSRs), memory, and I/O
- Go/halt processor run control
- Single step by assembly instruction
- Unlimited software breakpoints
- Real-time on-chip trace standard and optional off-chip trace
- On-chip trace depth 128 x 64-bit frames
- Off-chip trace depth 64K x 64-bit frames
- Support for System Management Mode (SMM), including single stepping through the transition to SMM
- Single step through real mode to protected mode transition while monitoring all register updates
- Flash programming support
- Hardware execution breakpoints using debug registers
- Trigger window for setting complex triggers
- Complex triggers can monitor address and cycle type
- Low-level access to JTAG functions
- Single line assembler and disassembler
- Trace window with full trace decode into instruction mnemonics
- Source window provides execution control: go, halt, go to cursor, step over/into call
- Source window can set or clear software or hardware breakpoints
- Interface driver for kernel level debugging with Windows CE Platform Builder and WinDbg with Windows XP/XPe debugging
- Command-line interface with Tcl/TK scripting language standard

### 5.2 Ethernet

The LX EPIC RDK's built-in Ethernet ports allow another debugging option. Ethernet-based debugging is supported by operating system development tools such as Eboot by Microsoft.

### 5.3 RS232

The ITE IT8712 SIO device provides two RS232/RS485 serial ports that can be used for serial debugging. BIOS setup may be required to utilize this functionality. RS232 serial debugging is supported by many software debugging tools such as the GNU Project Debugger (GDB).

## 6.0 Thermal Management

The ITE IT8712 SIO device provides the thermal monitoring interface for the LX EPIC RDK. The RDK provides a fan connector (J11), which supports speed control via a PWM output from the IT8712, as well as tachometer feedback to the IT8712 to monitor fan speed. A jumper (J27) allows the voltage level for the fan connector to be set to either 5V or 12V.

The RDK contains an on-board thermal sensor to monitor board temperature. This sensor input is monitored by the IT8712, which may then send an alarm signal to the CS5536 companion device if the temperature passes a programmed threshold level. This alarm signal generates an NMI that can be used for emergency power-down to help prevent system overheating.

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