



AMD Geode™ LX EPIC RDK Reference Schematic

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NOTES:

- 1) UNLESS OTHERWISE SPECIFIED RESISTORS HAVE 5% TOLERANCE.
- 2) UNLESS OTHERWISE SPECIFIED CAPACITORS HAVE 20% TOLERANCE.

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IMPORTANT NOTES ABOUT THIS SCHEMATIC

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

1) DESIGN NOTES in grey are information notes.

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

2) DESIGN NOTES in yellow are notes of caution.

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

3) DESIGN NOTES in red are critical, and must be understood and followed.


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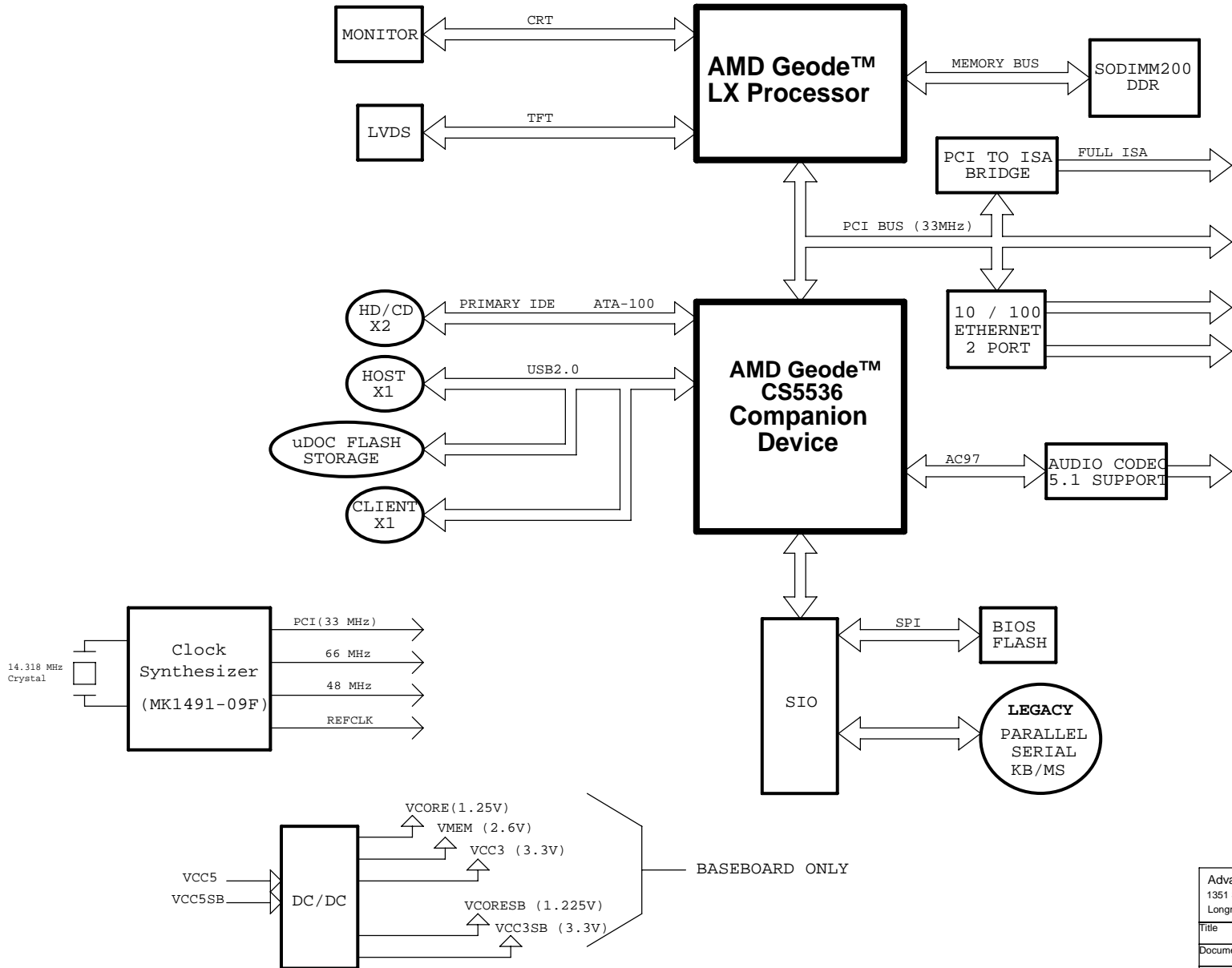
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REVISION HISTORY:

REV	DATE	NOTES
A	07-09-2006	* Initial Release
B	12-04-2006	* Page 8 - Changed LX symbol - DRGB6 pin from Y32 to AH8
C	01-19-2007	* Page 10 - Connected C102-C108 to Ground * Page 13 - Connected C133-C137 and C149-C152 to Ground
D	04-10-2007	* Page 13 - Added design note regarding USB VCORE supply.

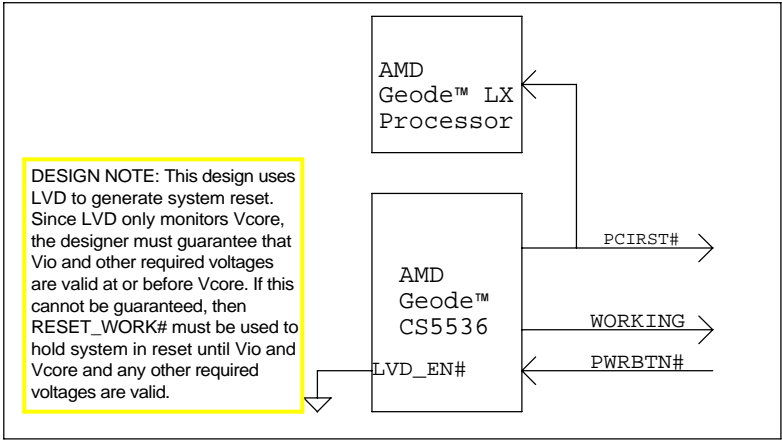
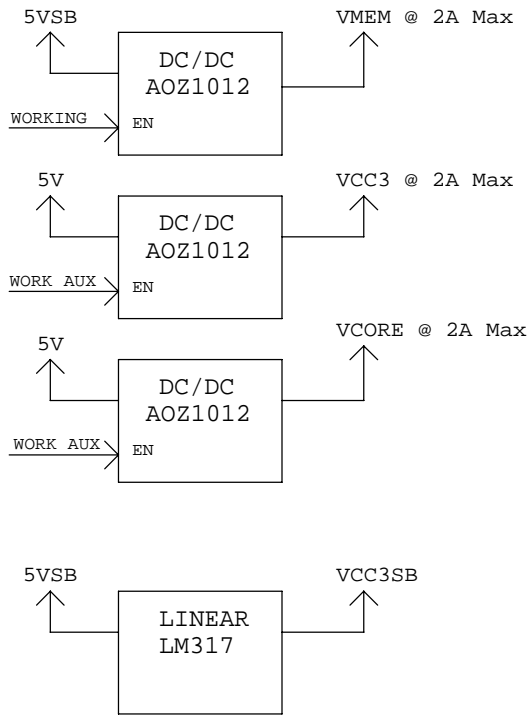
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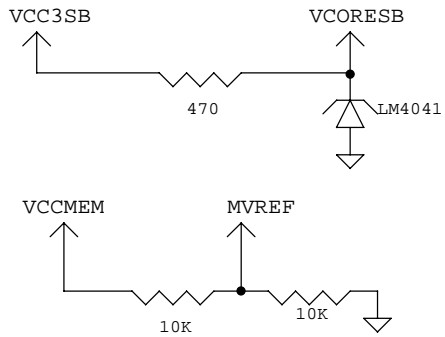
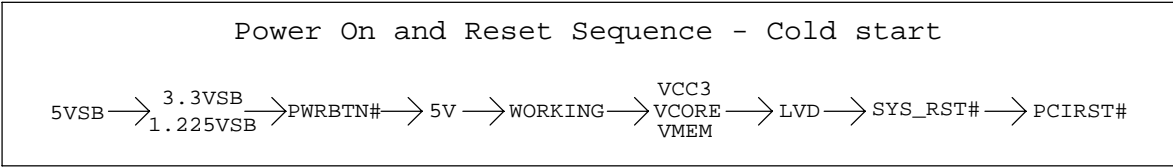


SYSTEM POWER
 VCC=+5.0V
 VCC3=+3.30V - BASEBOARD
 VCC3_EXT=+3.30V - PC104 SLOTS

AMD Geode™ LX Processor
 VCORE=+1.25V
 VCCMEM=+2.60V
 MVREF=+1.3V
 VIO=+3.30V

AMD Geode™ CS5536
 VCORE=+1.25V
 VCORESB=+1.225V
 VIO=+3.30V

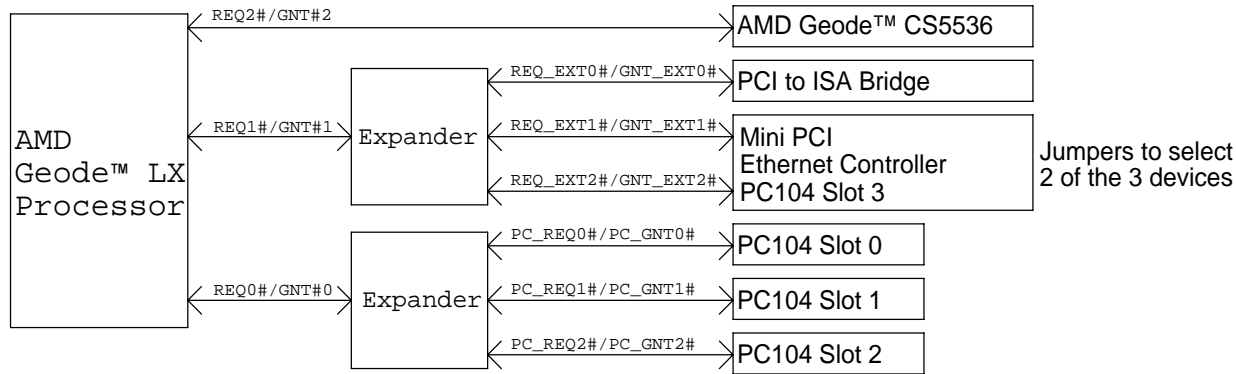
MEMORY
 VMEM=+2.60V
 MVREF=+1.3V



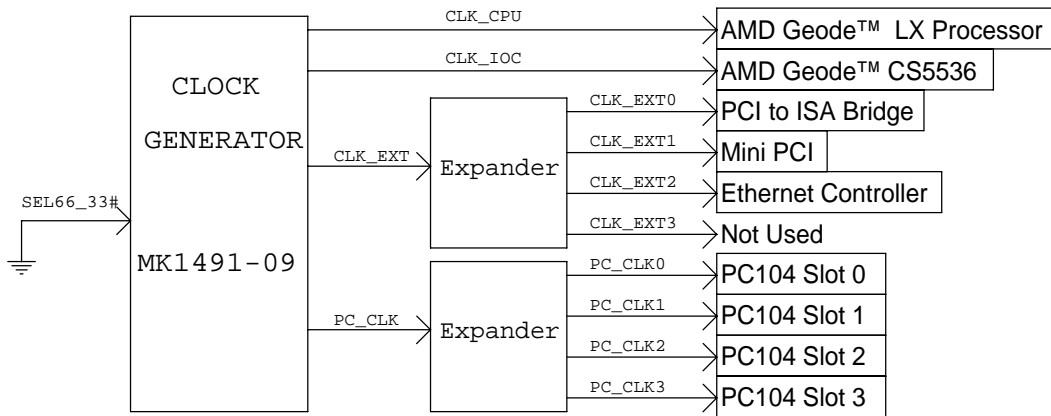
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PCI MASTER SETTING

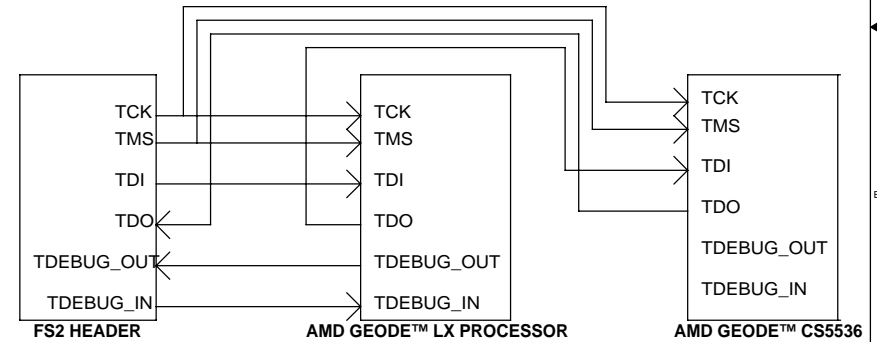


PCI CLOCK SETTING



SEL66_33#	Function
1	PCI 66 MHz
0	PCI 33 MHz

JTAG DAISY CHAIN MODE WITH AMD GEODE™ CS5536 COMPANION DEVICE

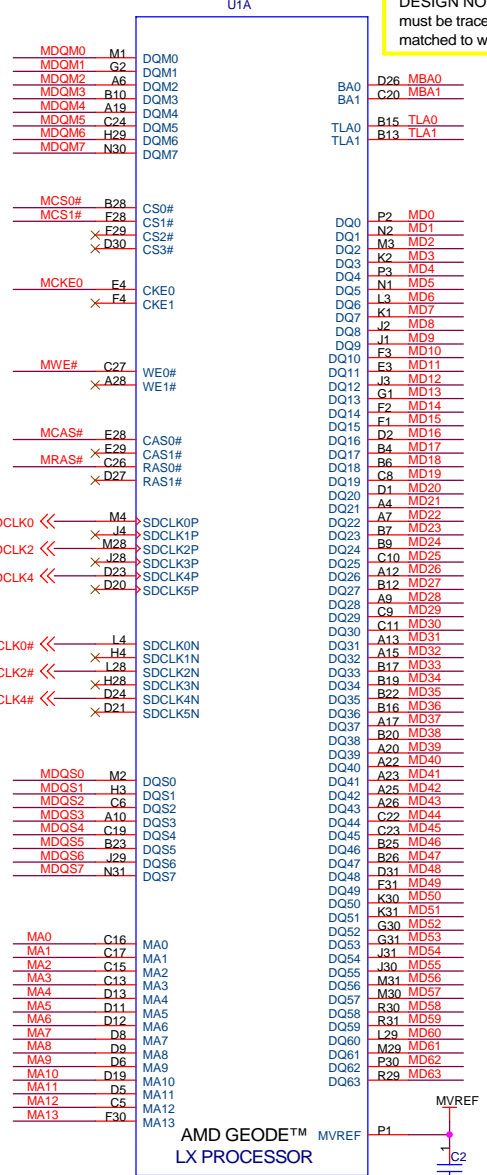


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DESIGN NOTE: See LX layout guidelines for latest recommendations on memory routing.

DESIGN NOTE: BA0,BA1 must be trace length matched to within 50 mils.



DESIGN NOTE: Use SDCLK pairs that are most convenient for clean routing.

DESIGN NOTE: Swap series resistors on the DQS lines in order minimize the number of vias.

DESIGN NOTE: Swap series resistors on the address lines in order minimize the number of vias.

DESIGN NOTE: Do not swap series resistors on the DQS, DQM or Data lines with the Address or control lines.

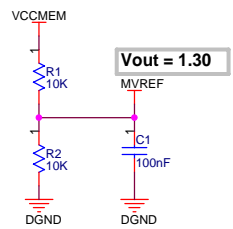
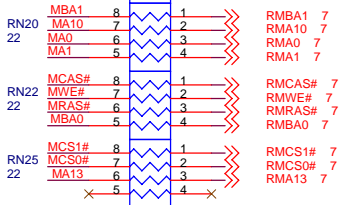
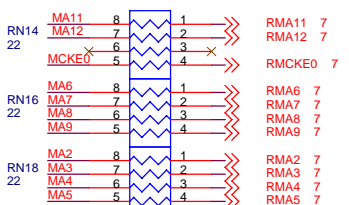
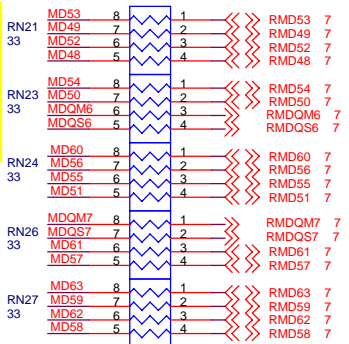
DESIGN NOTE: Swap series resistors on the data lines in order minimize the number of vias.

DESIGN NOTE: Place data bus series resistors as close to the memory devices as possible.

DESIGN NOTE: Place DQS and DQM series resistors as close to the SODIMM connector as possible.

DESIGN NOTE: This schematic shows a non-parallel terminated DDR solution. There may be restrictions as to the total number of DRAMs and the number of banks supported on the SODIMM. See LX layout guidelines for current restrictions.

DESIGN NOTE: Place address and control series resistors as close to the processor as possible.



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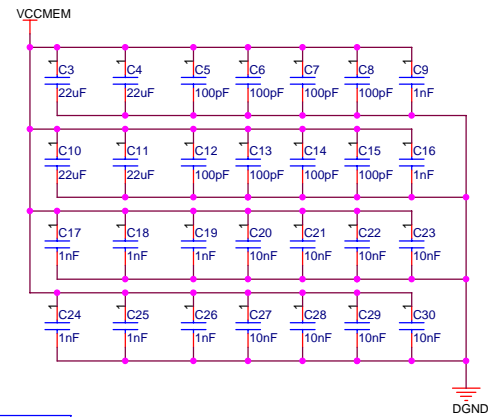
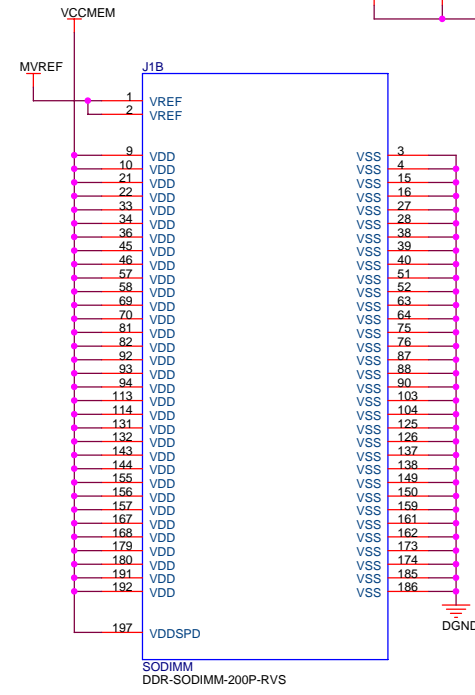
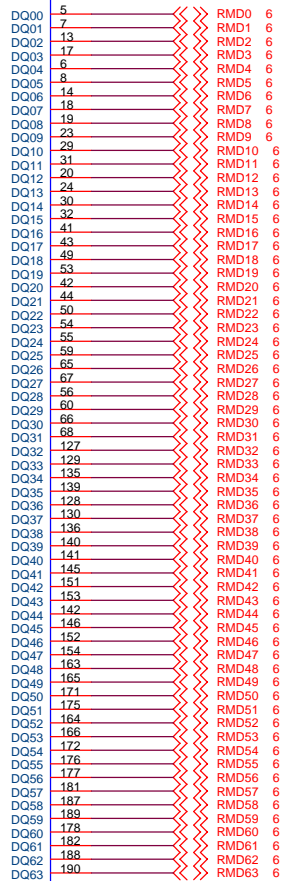
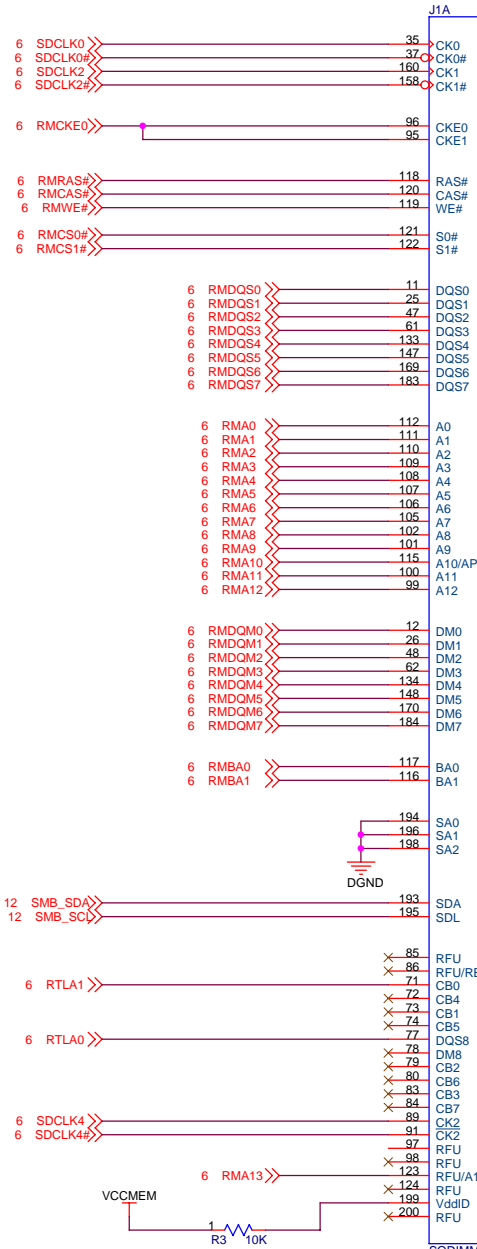
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DESIGN NOTE: This schematic shows a non-parallel terminated DDR solution. There may be restrictions as to the total number of DRAMS and the number of banks supported on the SODIMM. See LX layout guidelines for current restrictions.

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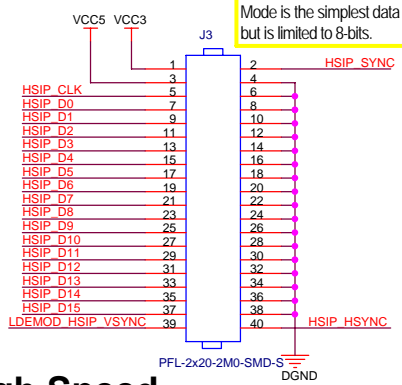
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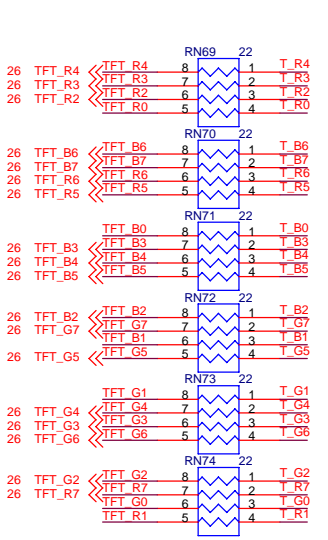
DESIGN NOTE: 8-bit Data Streaming Mode is the simplest data input mode, but is limited to 8-bits.



High Speed Input Port

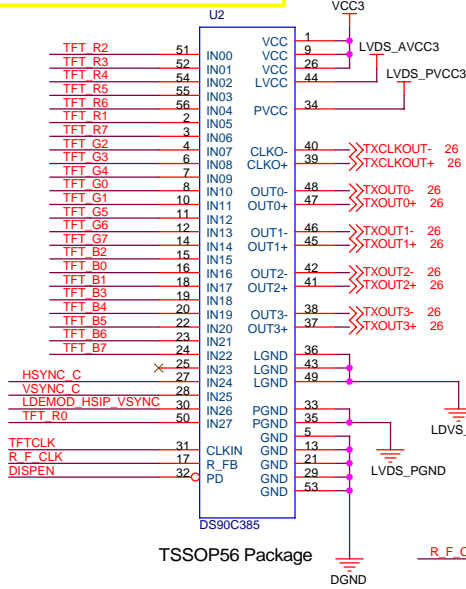
DESIGN NOTE: When using 16 data capture mode (Mode 4 - BT.601), the TFT interface cannot be used due to pin sharing conflicts.

DESIGN NOTE: There are two conventions for connecting 24 bit panels. One is backward compatible with 18 bit panels. The connections defined here are backwards compatible.

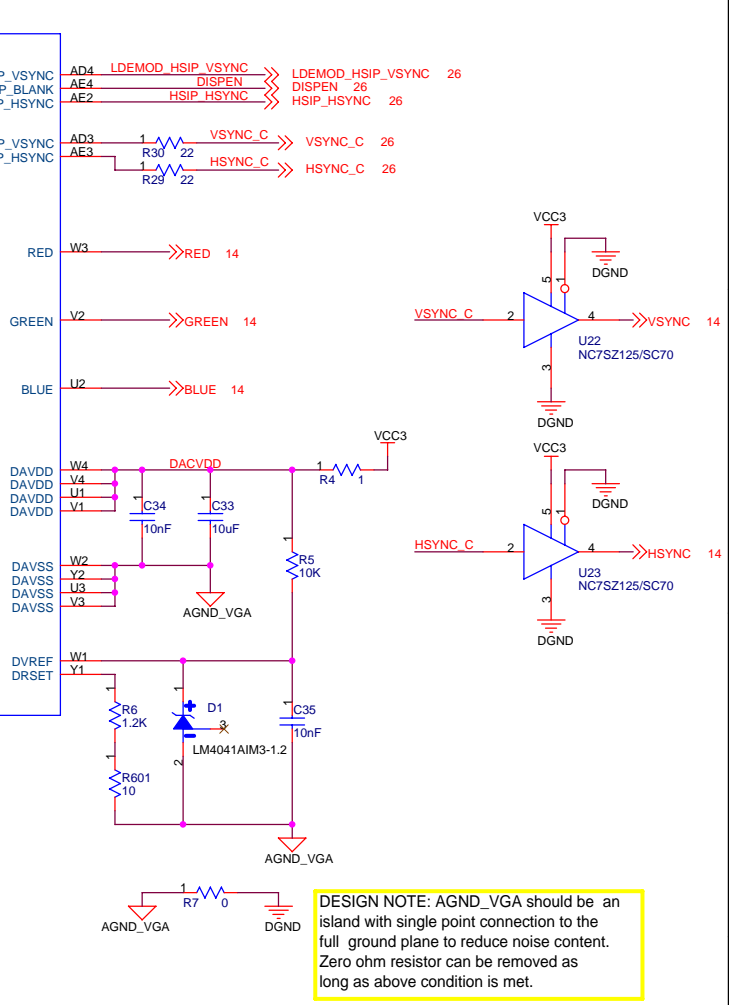
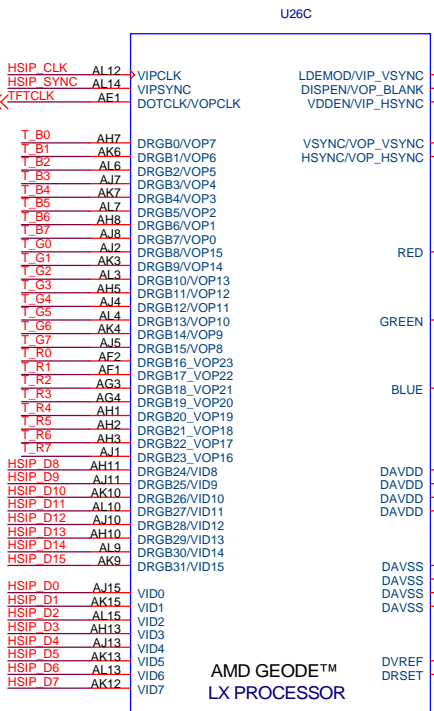
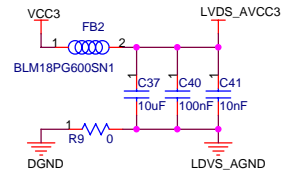
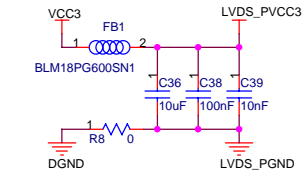


DESIGN NOTE: The LSB's for each color (R0,R1,G0,G1,B0,B1) are not used in by 18-bit panels.

DESIGN NOTE: For 18-bit panels use OUT0, OUT1, and OUT2. For 24-bit panels use OUT0, OUT1, OUT2, and OUT3.



24-bit LVDS Transmitter



DESIGN NOTE: AGND_VGA should be an island with single point connection to the full ground plane to reduce noise content. Zero ohm resistor can be removed as long as above condition is met.

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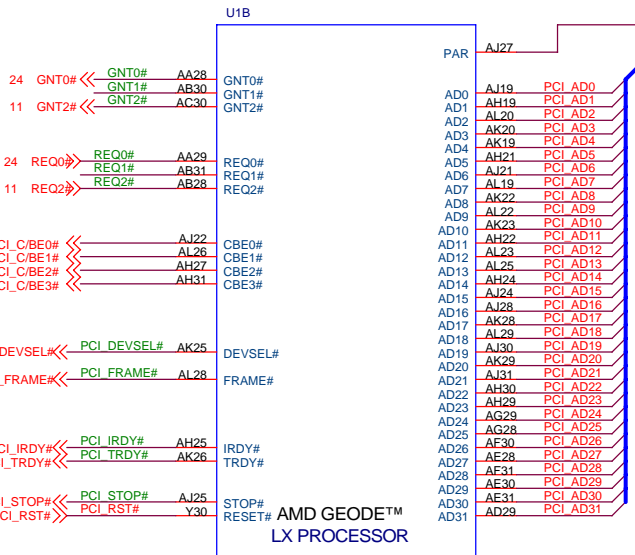
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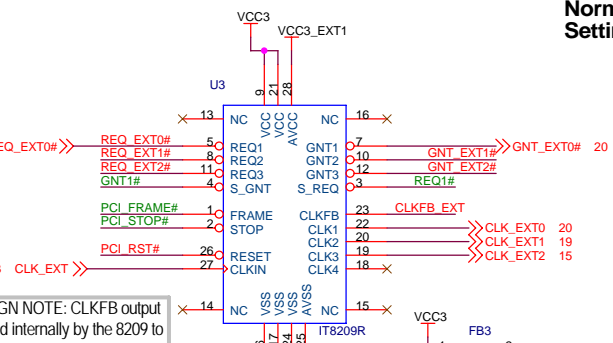
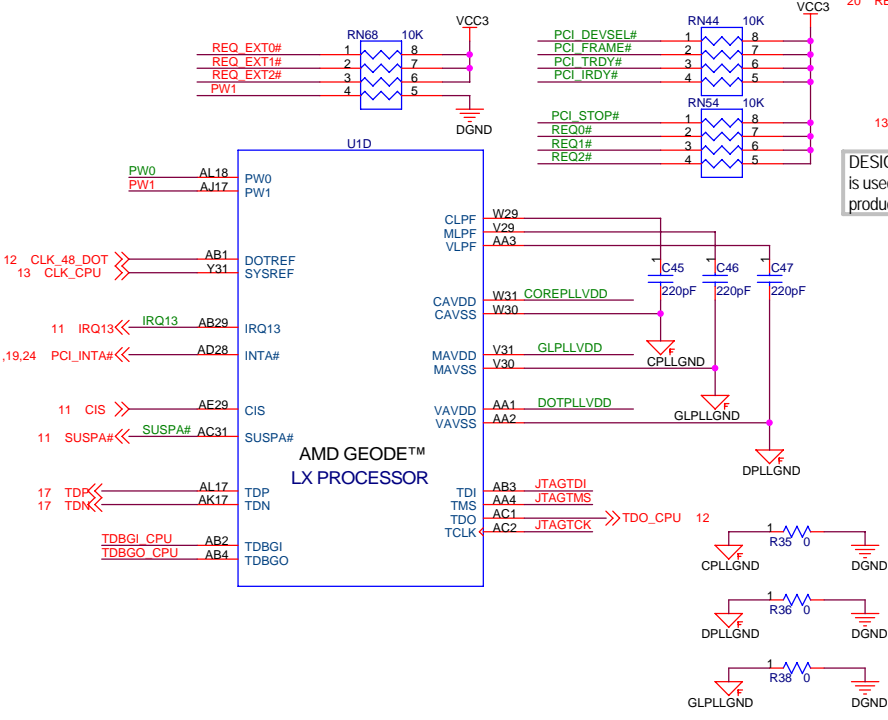
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DESIGN NOTE: There are 8 PCI devices in this design requiring REQ / GNT pairs. Two 1 to 3 expanders are provided, giving a total of 7 pairs. Two pairs are mapped to the following three devices: Ethernet, MiniPCI and PC104 slot 3. Jumpers are provided to select.

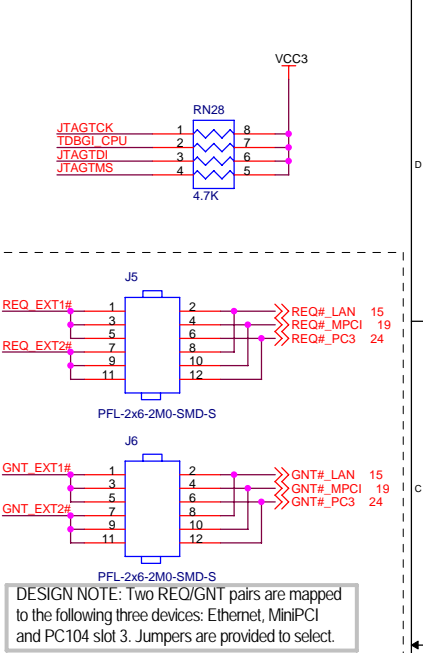
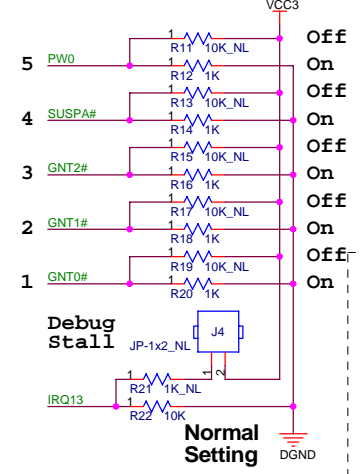


5	4	3	2	1	CORE	MEM
Off	On	Off	Off	Off	500	400
Off	On	Off	Off	On	500	333
Off	On	On	On	On	433	333
On	On	On	On	On	Bypass	Bypass

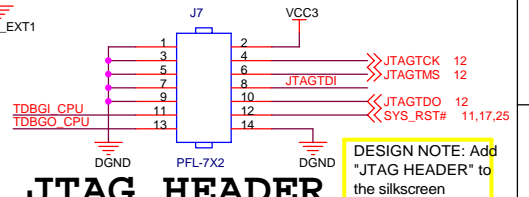


DESIGN NOTE: CLKFB output is used internally by the 8209 to produce the zero delay.

DESIGN NOTE: COREPLLVD, DOTPLLGD and GLPLLGD should each be an island with single point connection to the full ground plane to reduce noise content. Zero ohm resistor can be removed as long as above condition is met.



DESIGN NOTE: Two REQ/GNT pairs are mapped to the following three devices: Ethernet, MiniPCI and PC104 slot 3. Jumpers are provided to select.



DESIGN NOTE: Add "JTAG HEADER" to the silkscreen

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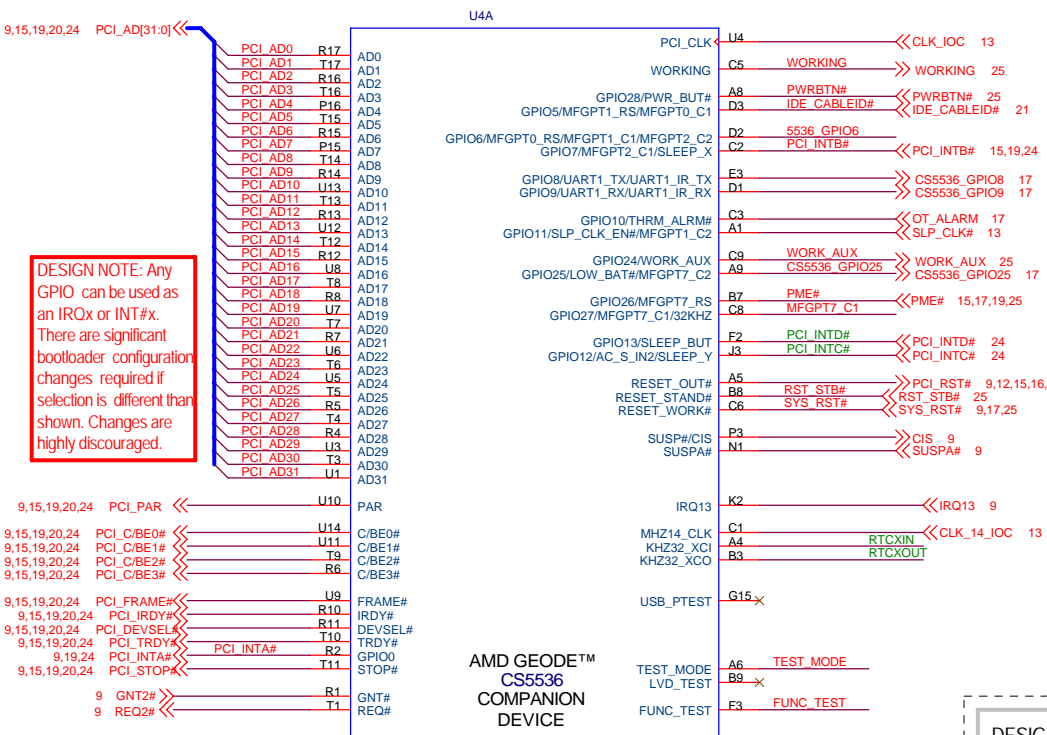
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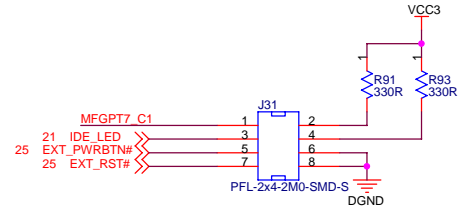
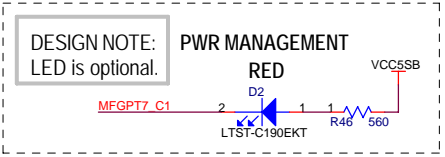
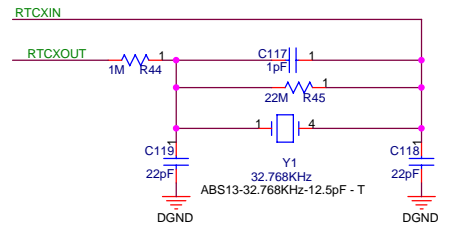
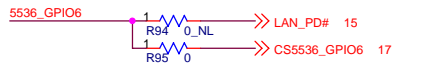
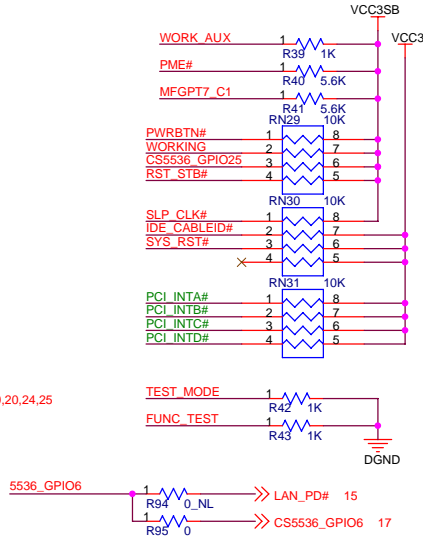
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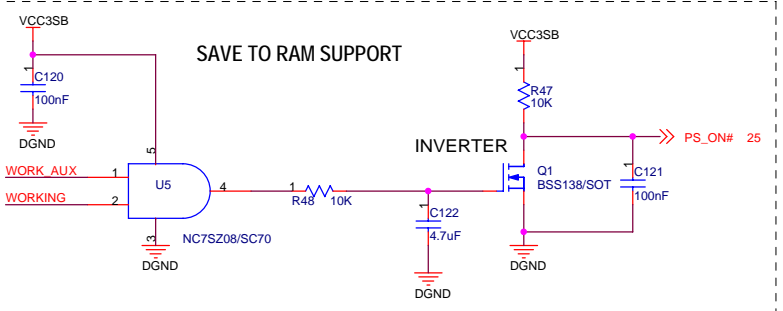
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DESIGN NOTE: Any GPIO can be used as an IRQx or INT#x. There are significant bootloader configuration changes required if selection is different than shown. Changes are highly discouraged.



DESIGN NOTE: GPIO24/WORK_AUX is an open drain output, which requires a pullup resistor to achieve a high state. At initial standby power application the GPIO24/WORK_AUX pin defaults to GPIO24 and the GPIO24 defaults as an input. This default combination will leave the pin in a high state due to the pullup which is normally connected to VCC3SB. This circuit works around that behaviour so that Save to RAM will function correctly.



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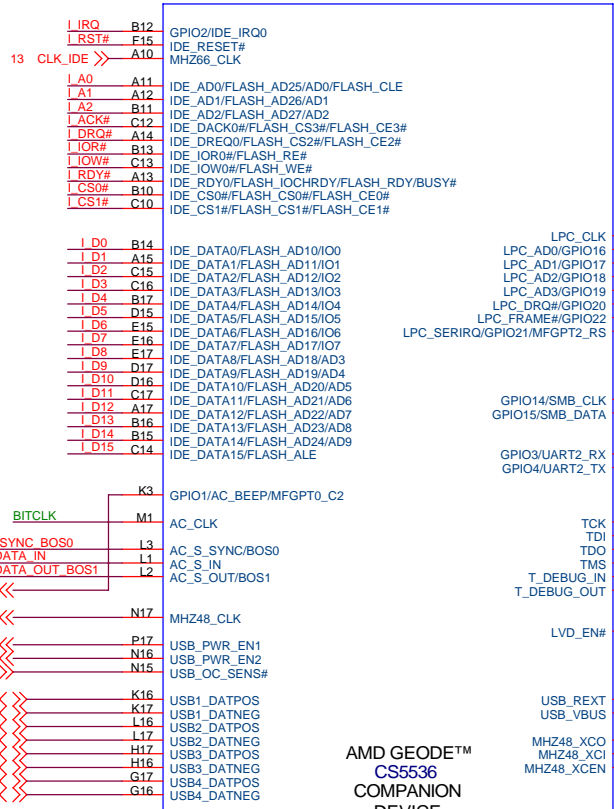
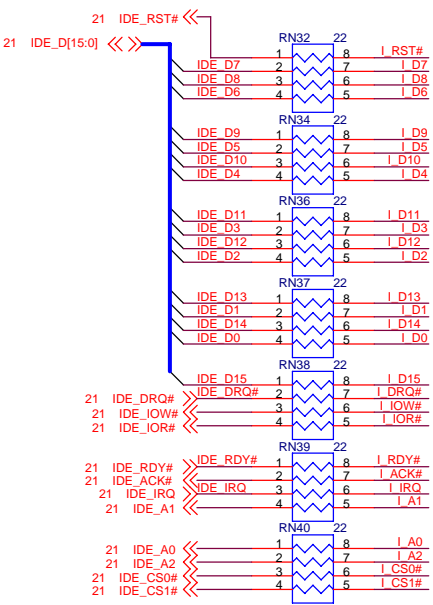
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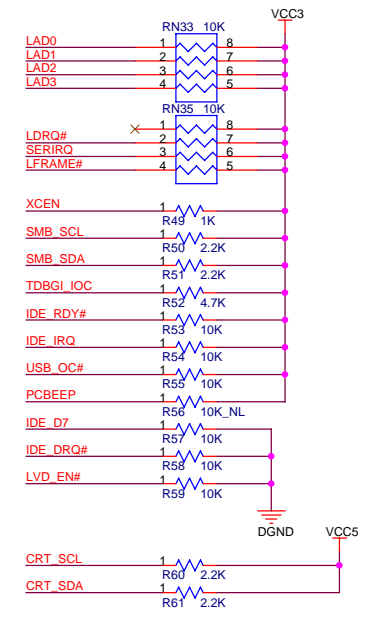
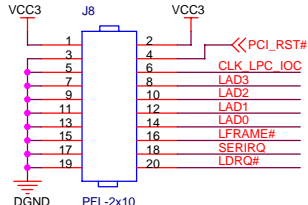
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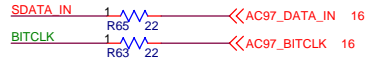
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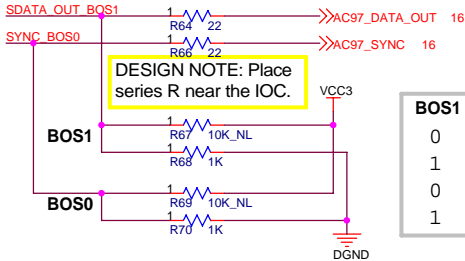
LPC Header



DESIGN NOTE: Place series R near the audio CODEC.



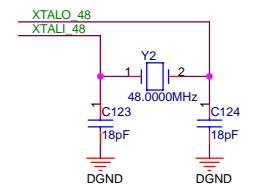
DESIGN NOTE: USBPWR_EN1/2 and USB_OC# are used for a fully compliant USB design. See Option Schematics for fully compliant USB design.



DESIGN NOTE: Place series R near the IOC.

BOS1	BOS0	BOOT STRAP OPTIONS
0	0	LPC ROM OFF LPC
1	0	NOR FLASH OFF IDE INTERFACE
0	1	RESERVED
1	1	SST FWH OFF LPC (DEFAULT)

DESIGN NOTE: This design uses LVD (LVD_EN# tied low) to generate system reset. Since LVD only monitors Vcore in the working domain, the designer must guarantee that Vio and other required voltages are valid at or before Vcore. If this cannot be guaranteed, then RESET_WORK# must be used to hold system in reset until Vio and Vcore and any other required voltages are valid.



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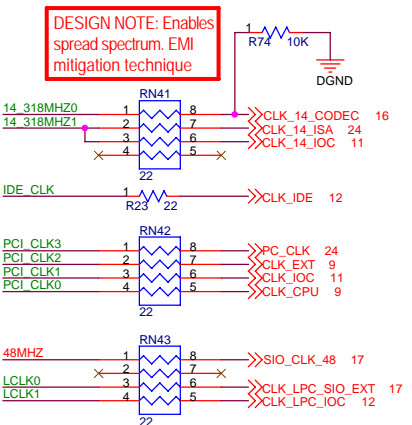
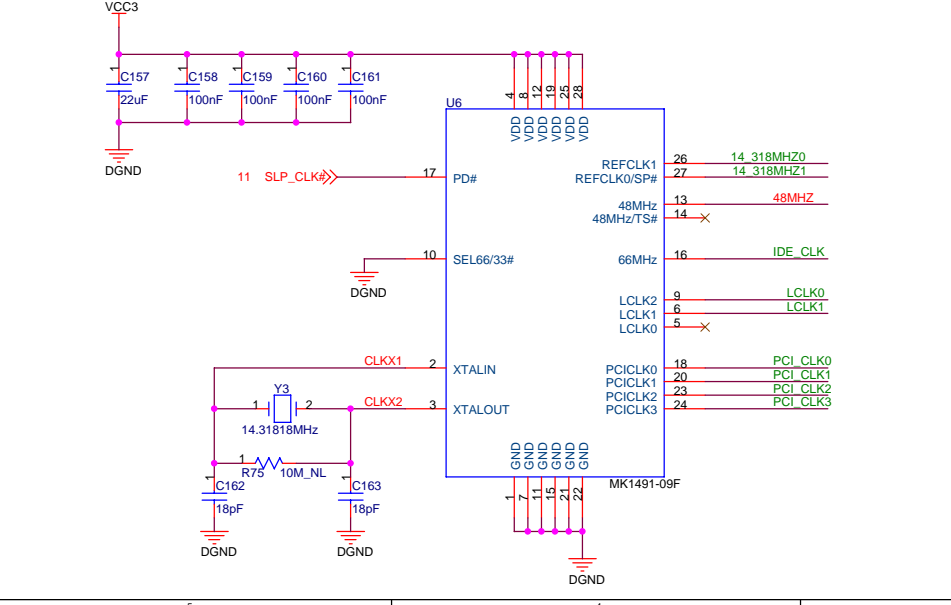
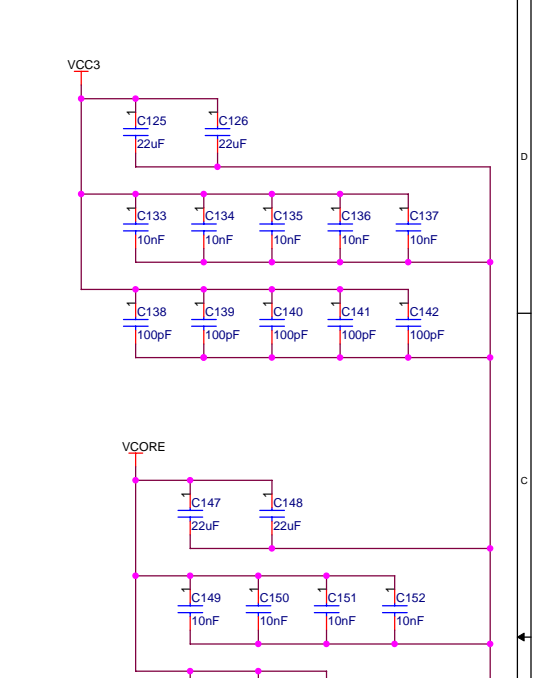
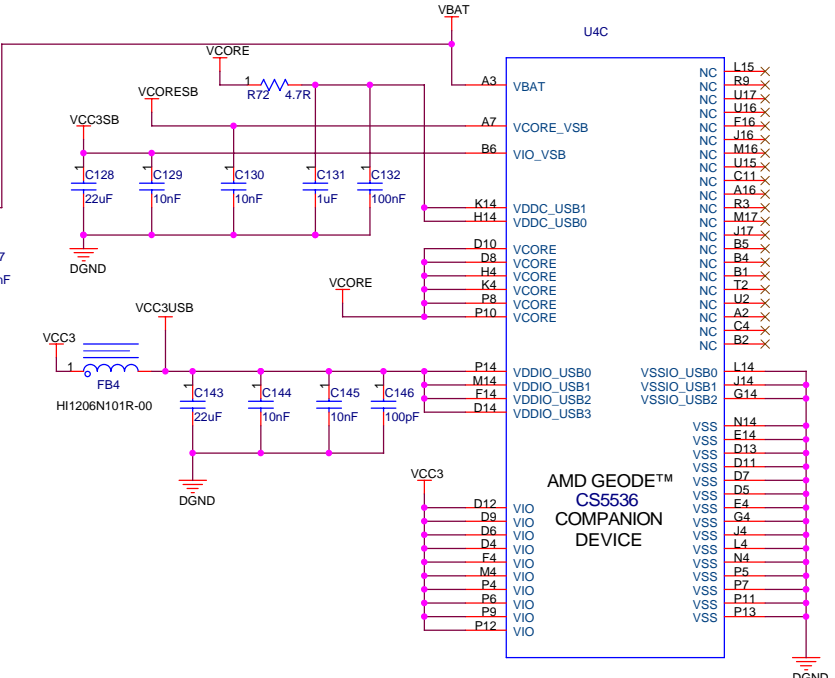
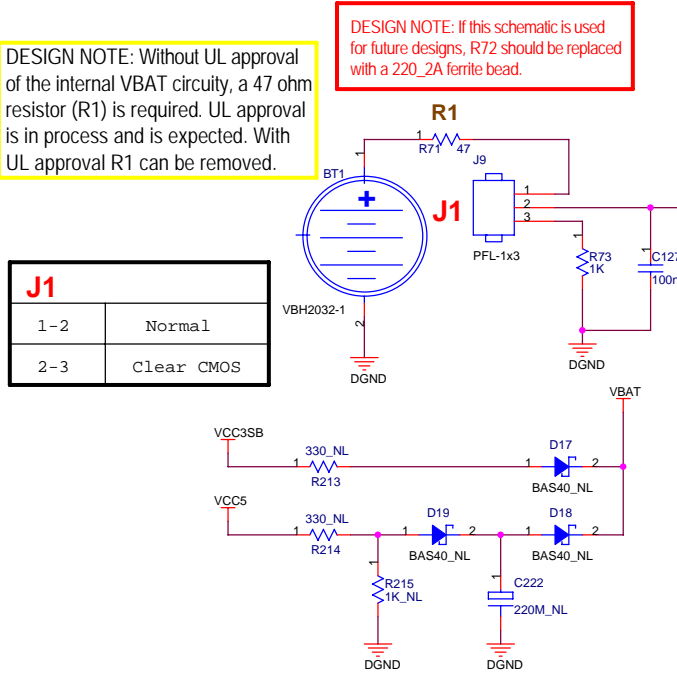
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DESIGN NOTE: Without UL approval of the internal VBAT circuitry, a 47 ohm resistor (R1) is required. UL approval is in process and is expected. With UL approval R1 can be removed.

DESIGN NOTE: If this schematic is used for future designs, R72 should be replaced with a 220_2A ferrite bead.

J1	
1-2	Normal
2-3	Clear CMOS



DESIGN NOTE: Swap series resistors on the clock lines in order minimize the number of vias.

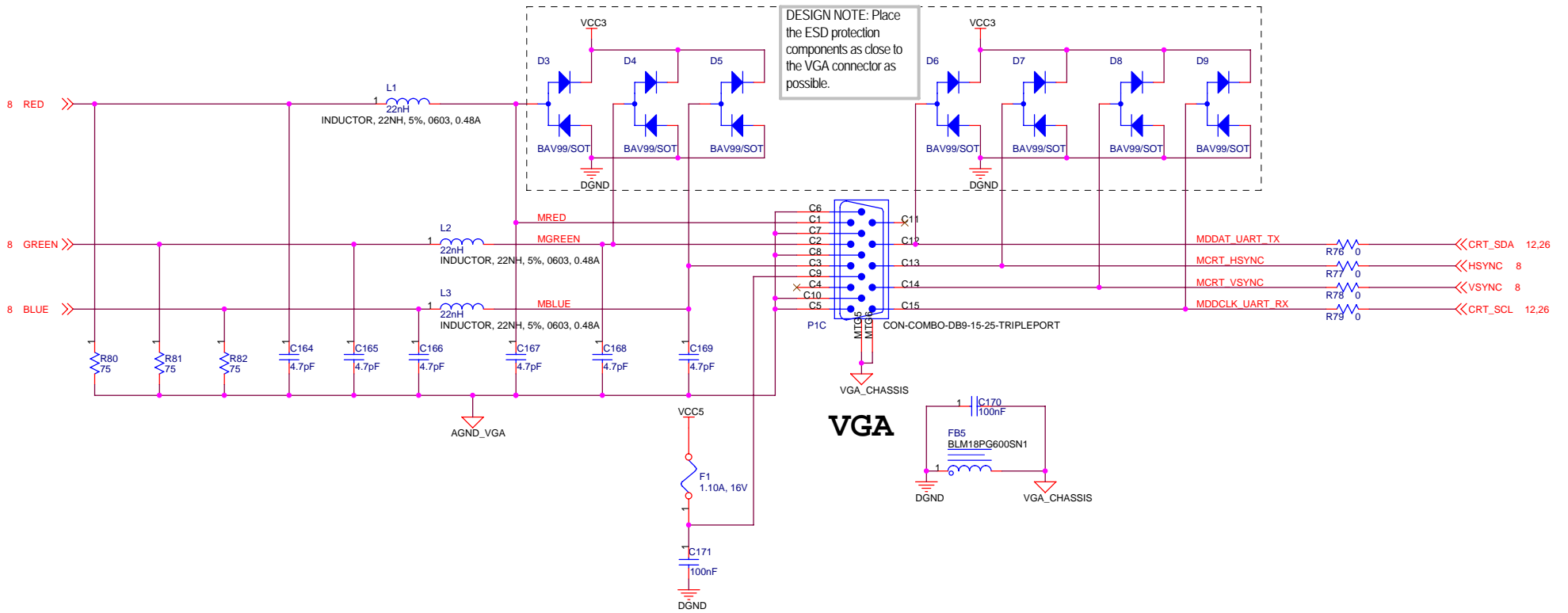
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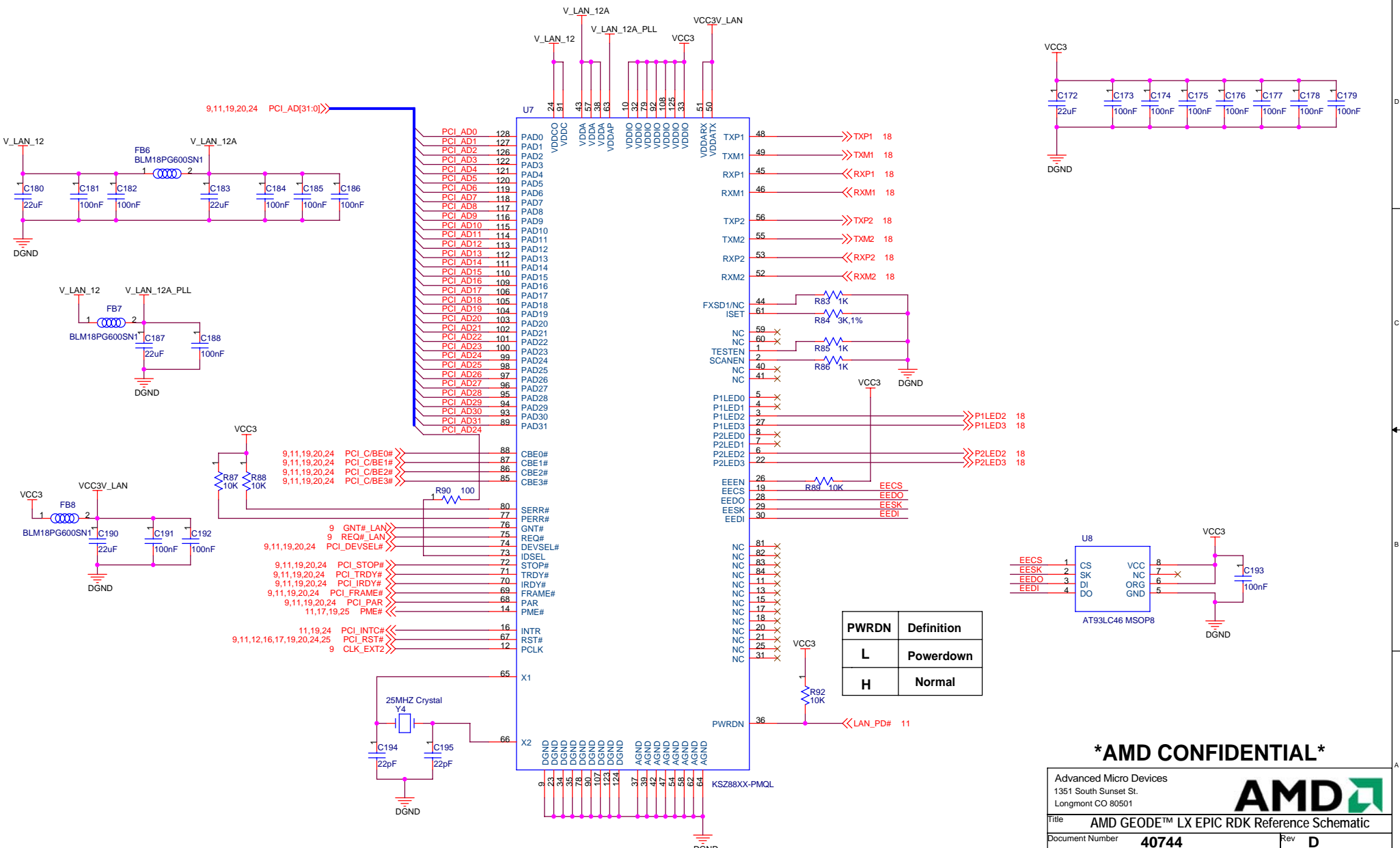
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PWRDN	Definition
L	Powerdown
H	Normal

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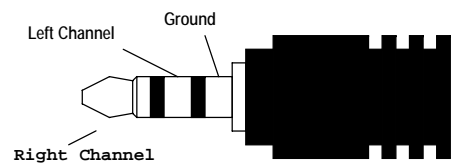
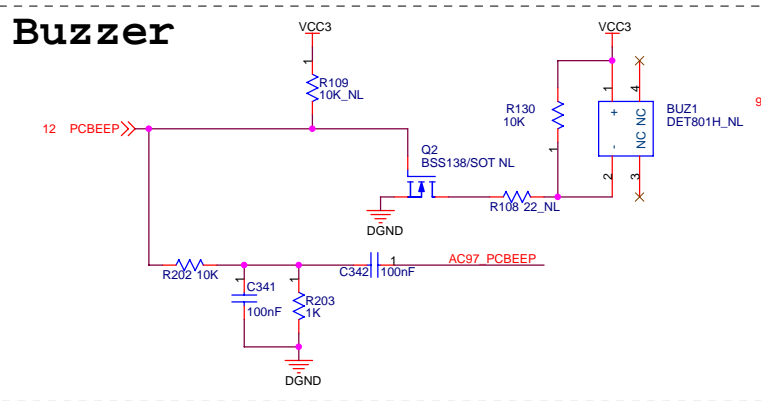
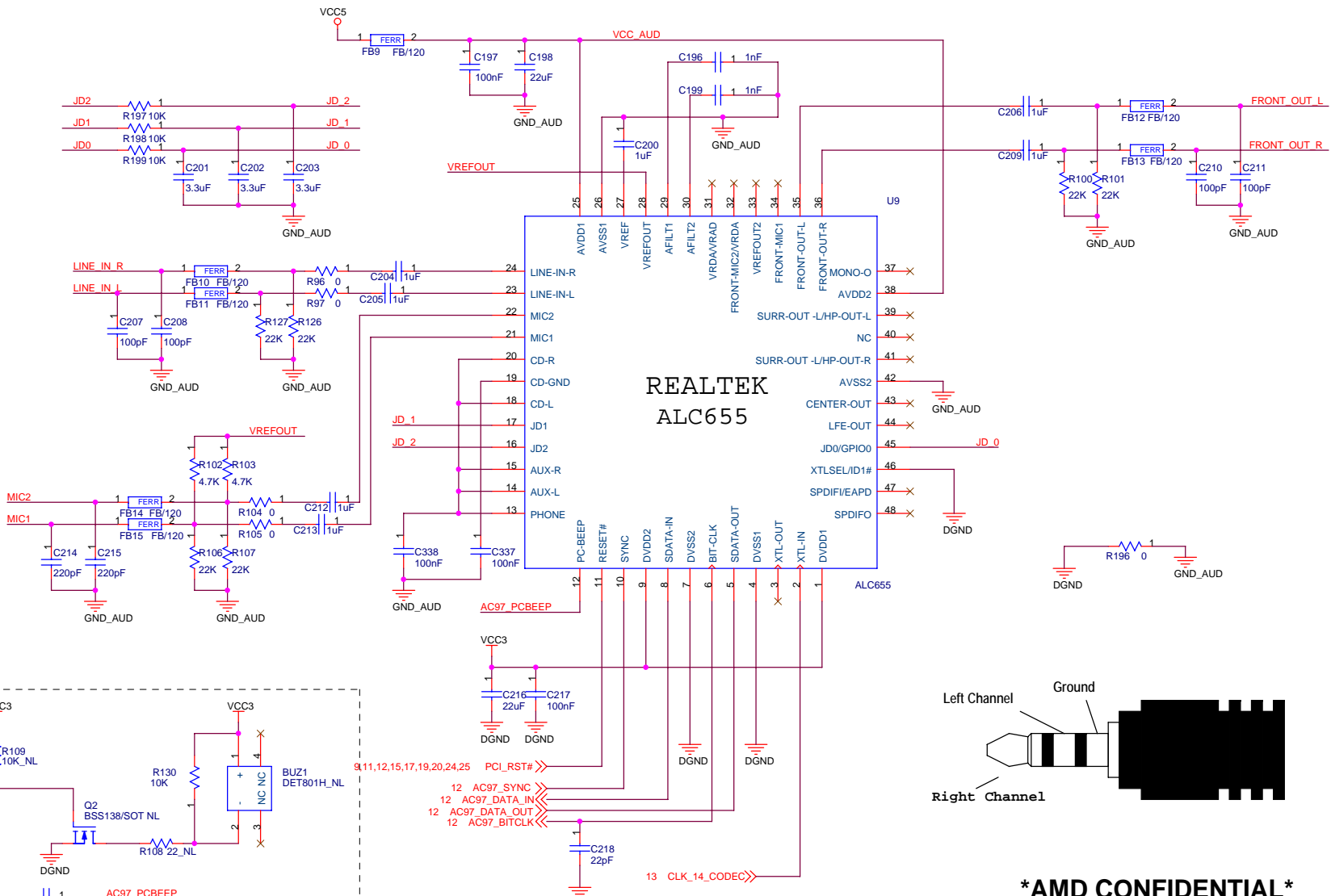
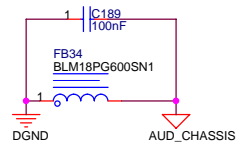
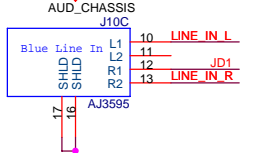
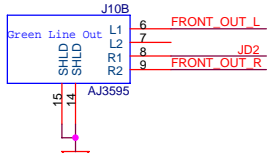
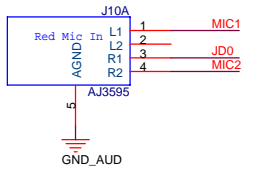
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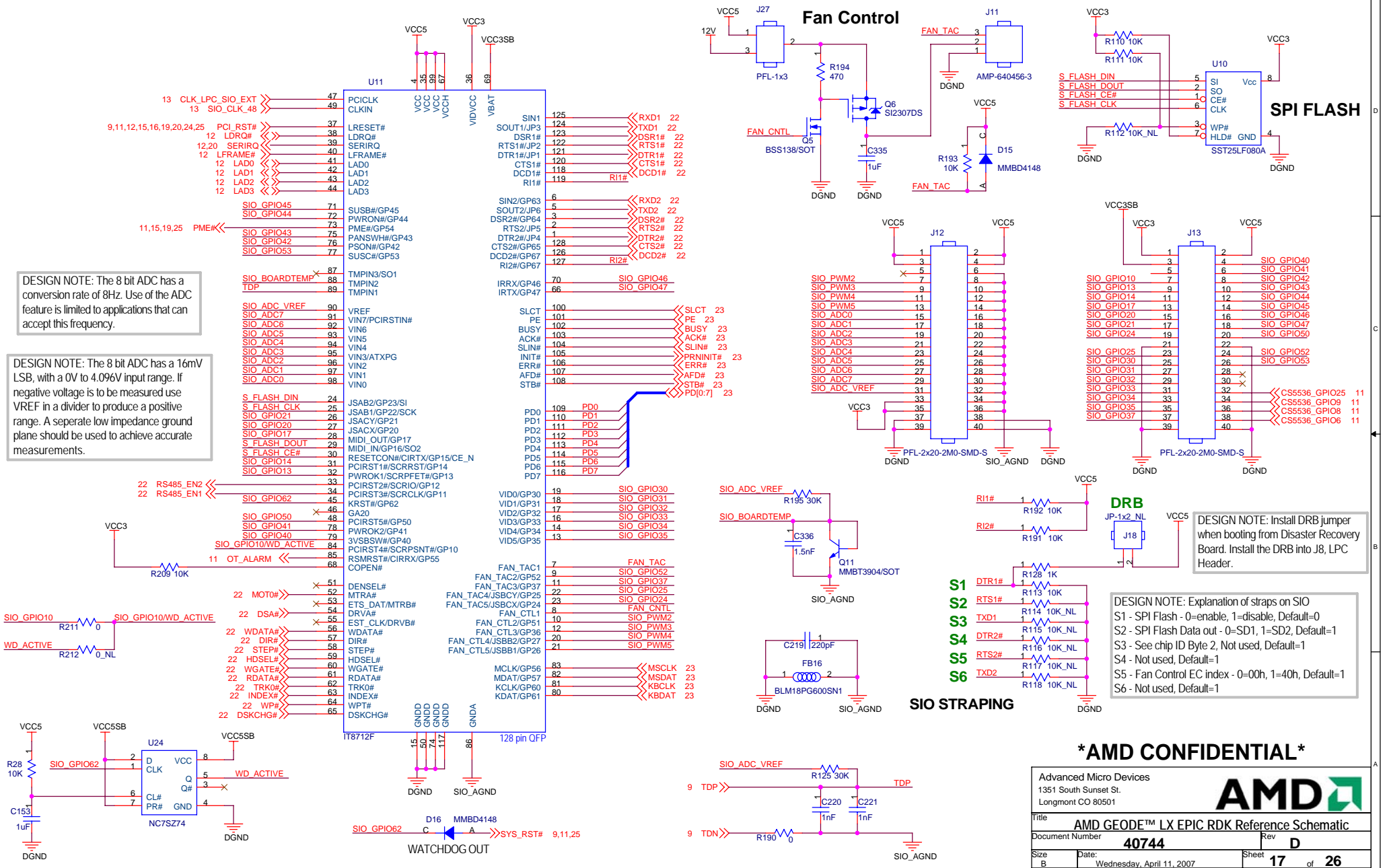
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DESIGN NOTE: Use 14.318MHz external clock

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DESIGN NOTE: The 8 bit ADC has a conversion rate of 8Hz. Use of the ADC feature is limited to applications that can accept this frequency.

DESIGN NOTE: The 8 bit ADC has a 16mV LSB, with a 0V to 4.096V input range. If negative voltage is to be measured use VREF in a divider to produce a positive range. A separate low impedance ground plane should be used to achieve accurate measurements.

DESIGN NOTE: Install DRB jumper when booting from Disaster Recovery Board. Install the DRB into J8, LPC Header.

DESIGN NOTE: Explanation of straps on SIO

- S1 - SPI Flash - 0=enable, 1=disable, Default=0
- S2 - SPI Flash Data out - 0=SD1, 1=SD2, Default=1
- S3 - See chip ID Byte 2, Not used, Default=1
- S4 - Not used, Default=1
- S5 - Fan Control EC index - 0=00h, 1=40h, Default=1
- S6 - Not used, Default=1

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DESIGN NOTE:
 Reg. SGR5 bit [15,9] = [1,0]
 LED3 = Act
 LED2 = Link

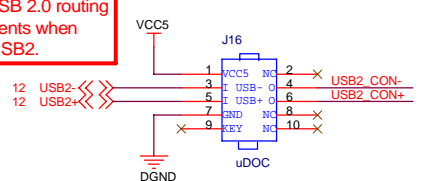
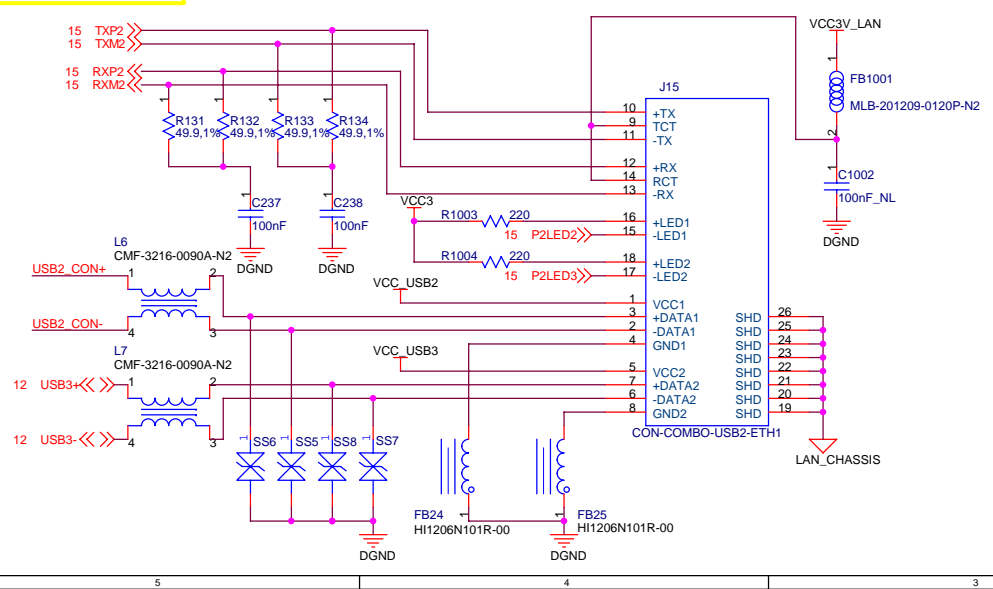
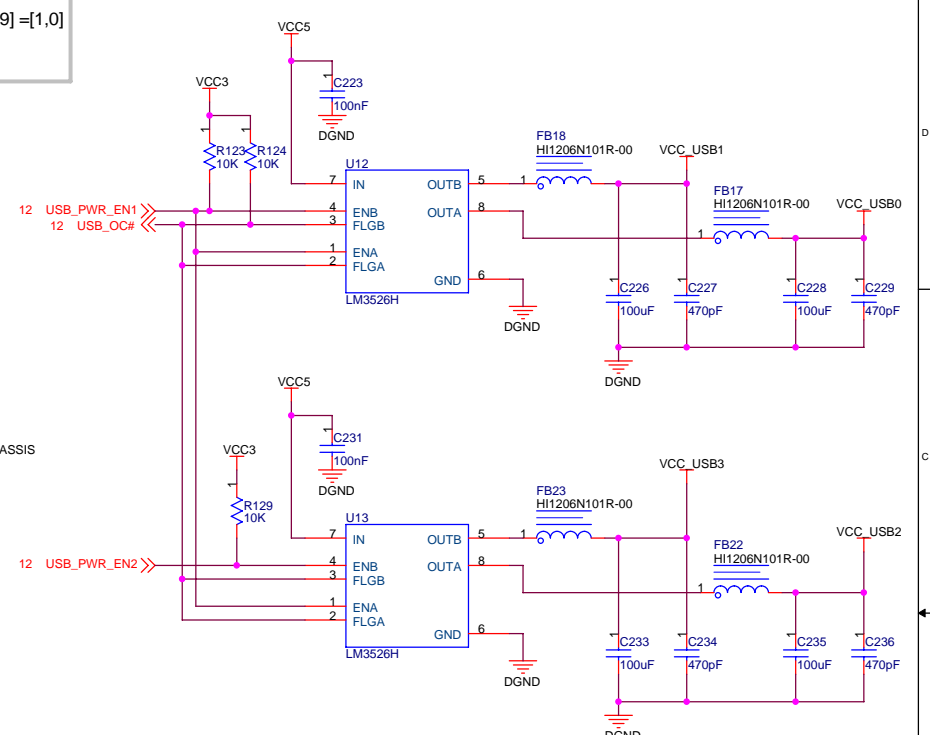
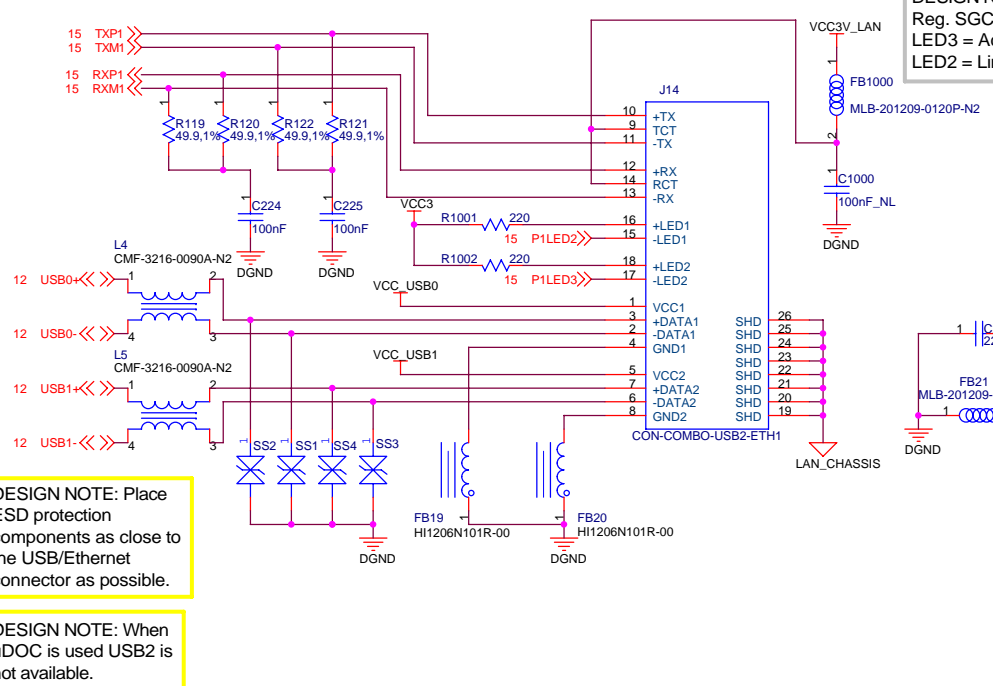
DESIGN NOTE: Place ESD protection components as close to the USB/Ethernet connector as possible.

DESIGN NOTE: When uDOC is used USB2 is not available.

DESIGN NOTE: Do not violate USB 2.0 routing requirements when routing USB2.

DESIGN NOTE: Jumper pins 3 & 4, 5 & 6 when uDOC is not used.

DESIGN NOTE: Pin 9 on header should be cut off.

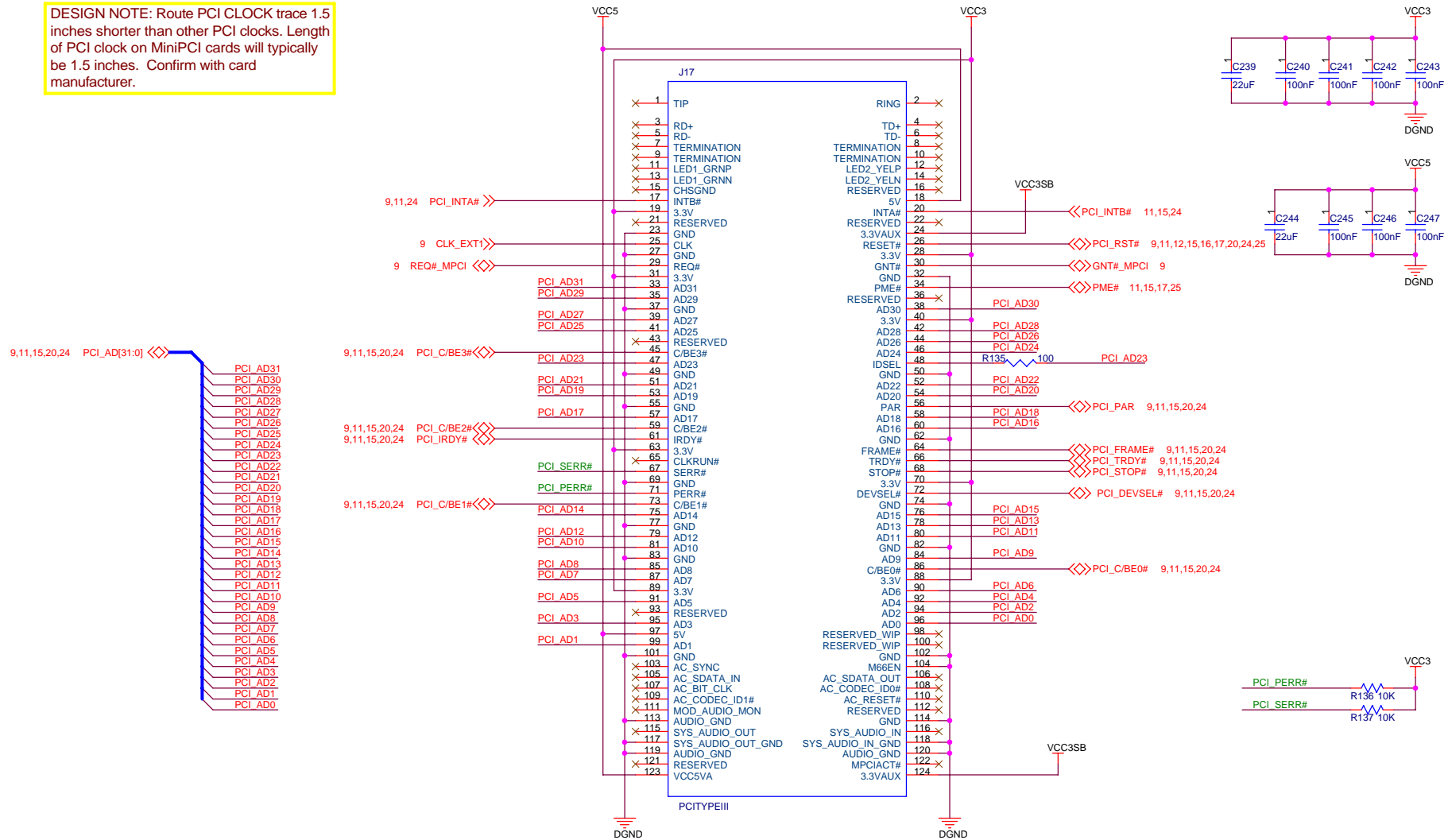


M-Systems uDOC Connector

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DESIGN NOTE: Route PCI CLOCK trace 1.5 inches shorter than other PCI clocks. Length of PCI clock on MiniPCI cards will typically be 1.5 inches. Confirm with card manufacturer.



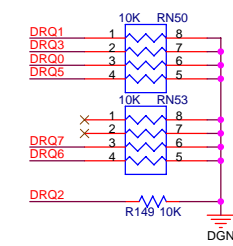
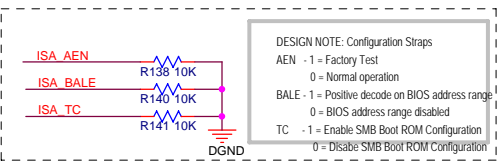
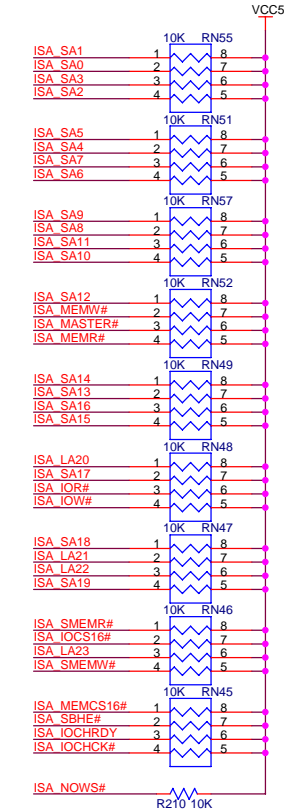
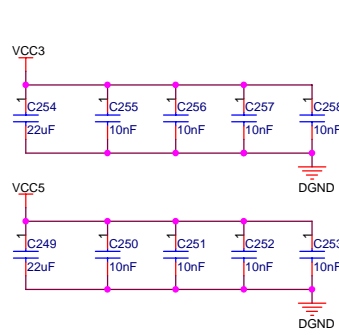
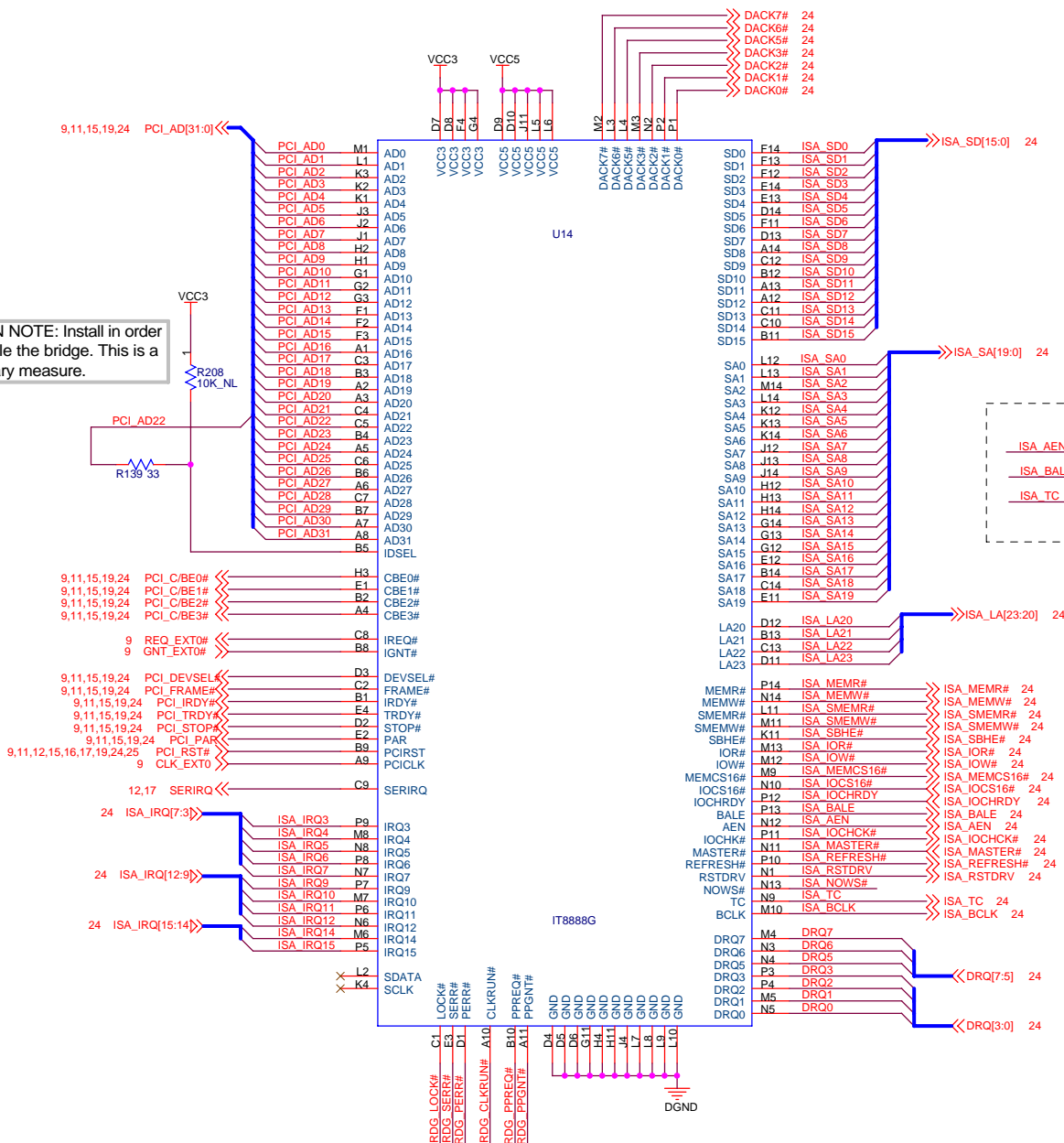
DESIGN NOTE: Consult MiniPCI card manufacturer for any special design or layout considerations of MiniPCI slot to accommodate a particular MiniPCI card.

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DESIGN NOTE: Install in order to disable the bridge. This is a temporary measure.



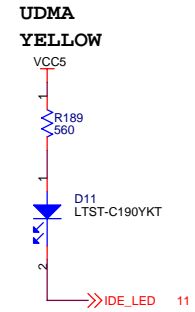
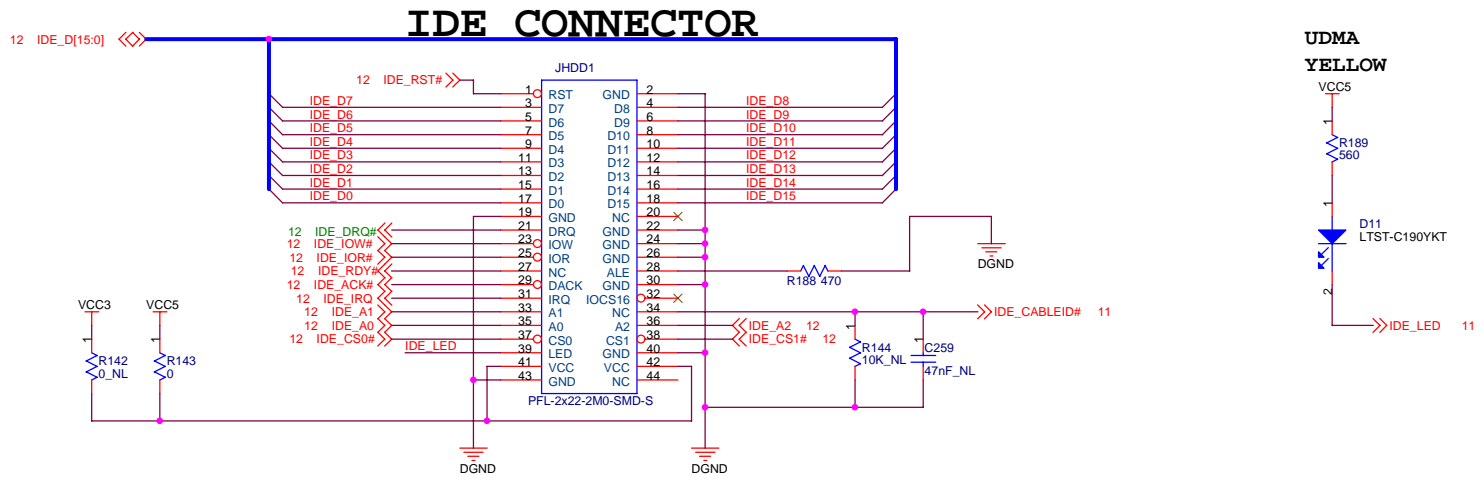
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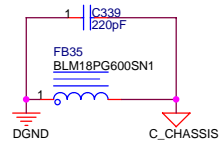
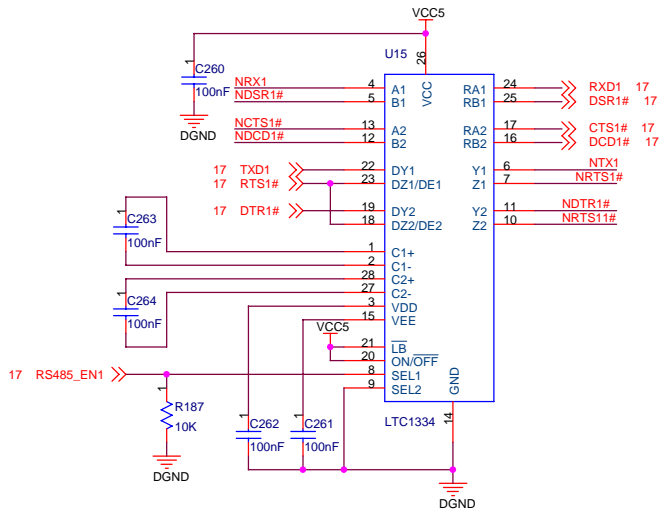
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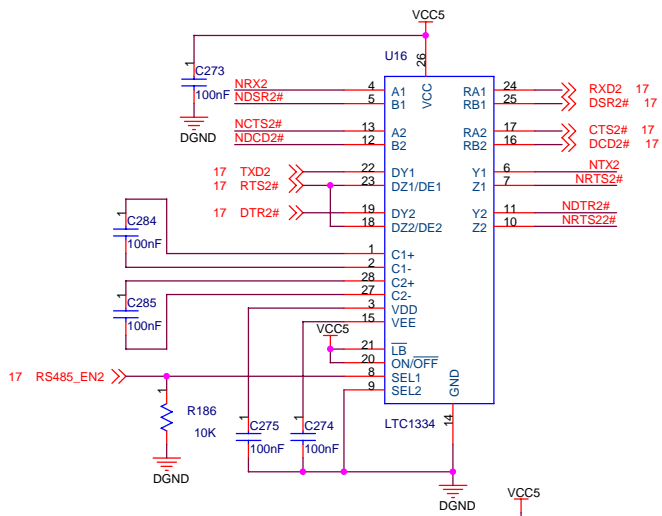
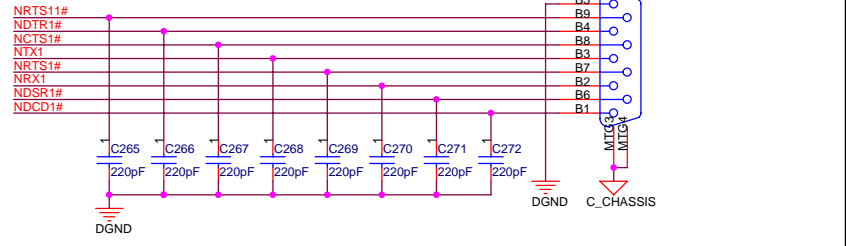


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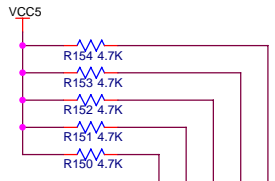
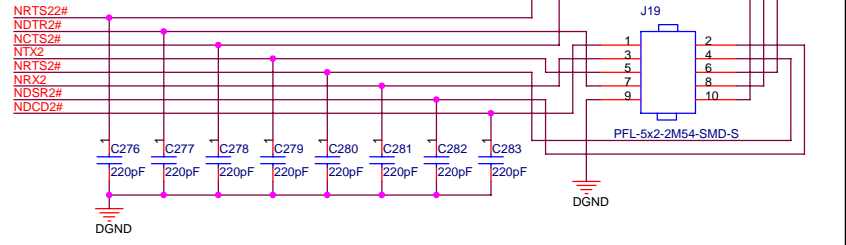
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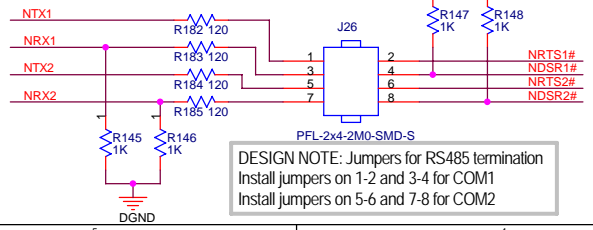
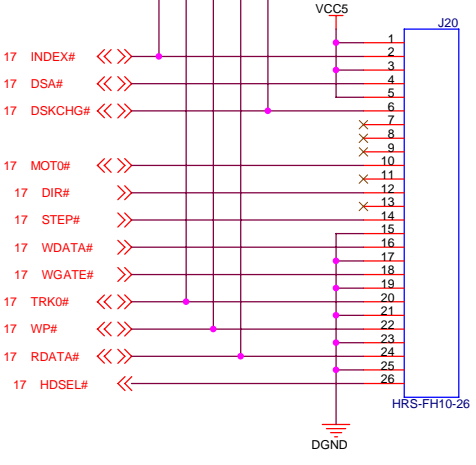
COM1



COM2



FDD CNT



DESIGN NOTE: Jumpers for RS485 termination
 Install jumpers on 1-2 and 3-4 for COM1
 Install jumpers on 5-6 and 7-8 for COM2

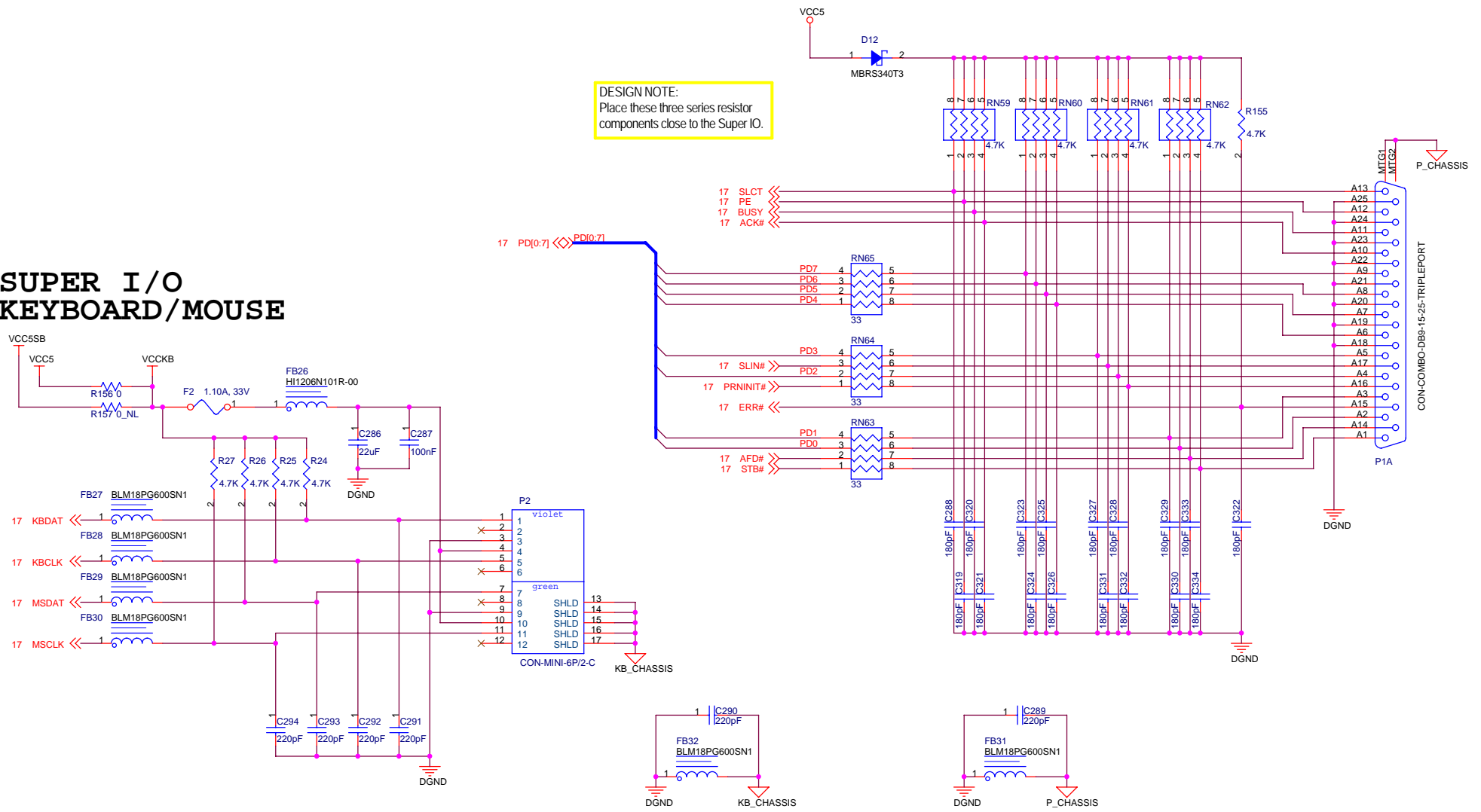
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SUPER I/O KEYBOARD/MOUSE

DESIGN NOTE:
Place these three series resistor
components close to the Super IO.

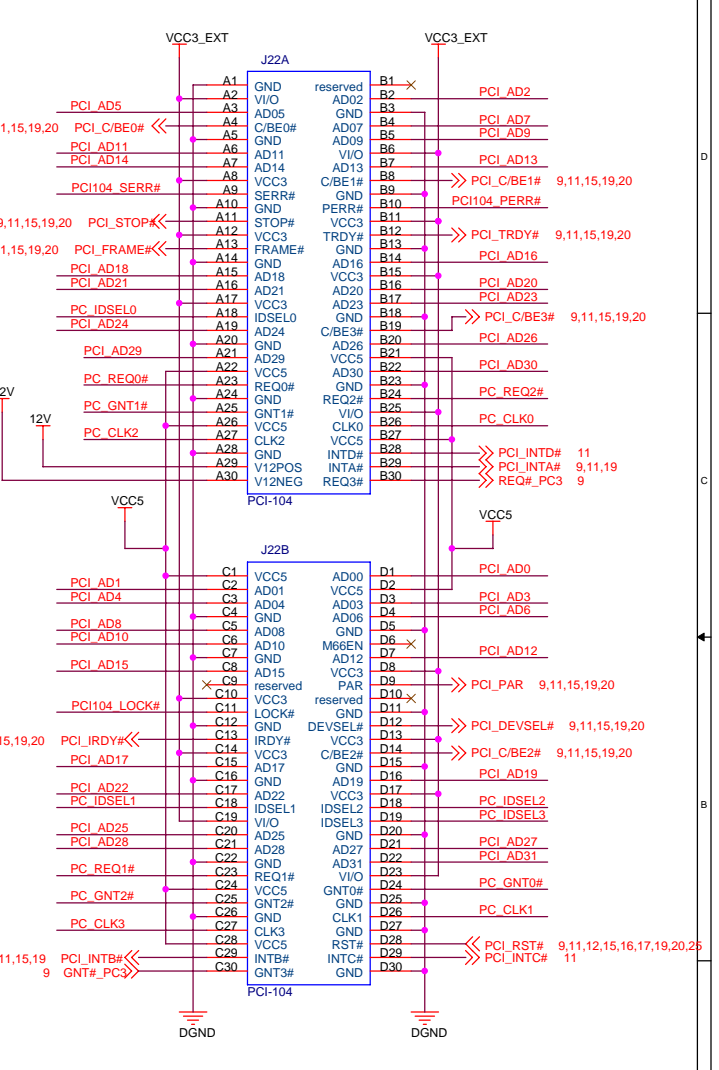
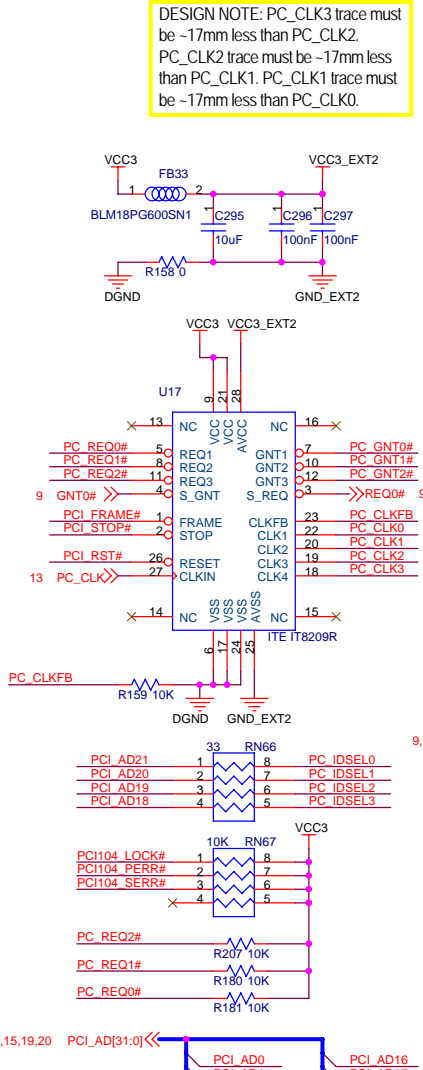
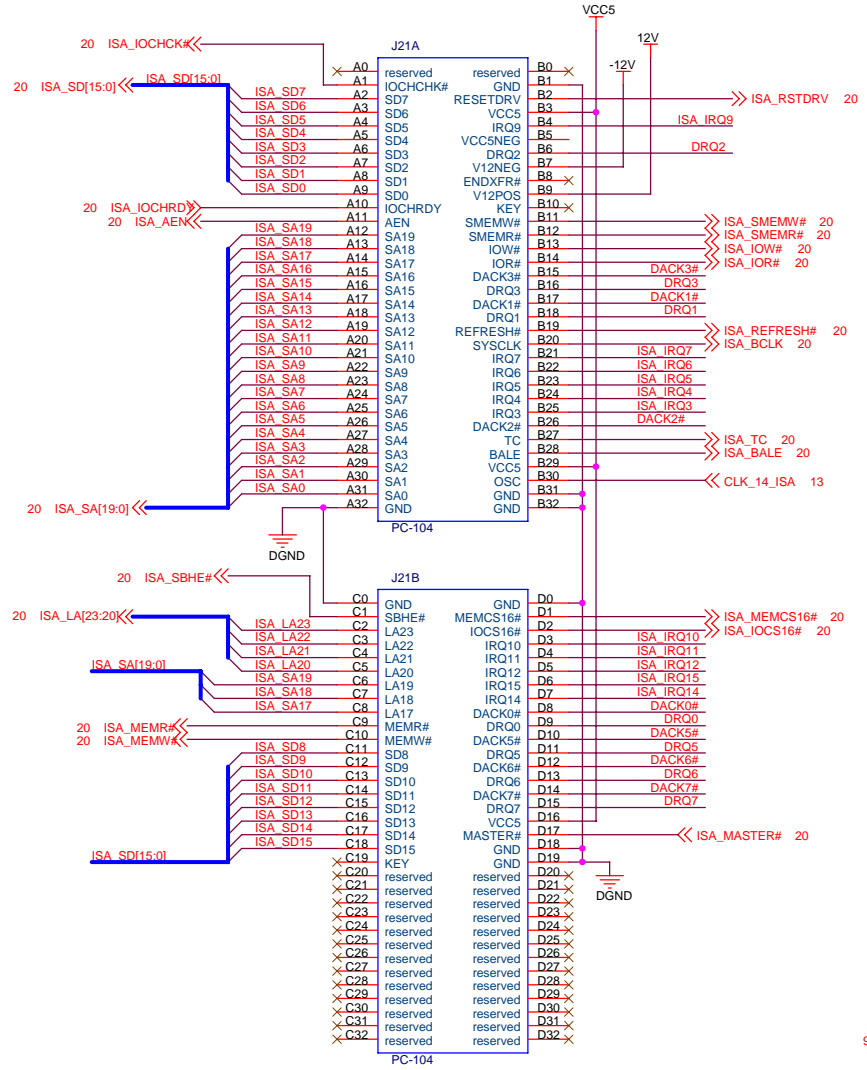


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DESIGN NOTE: PC_CLK3 trace must be ~17mm less than PC_CLK2. PC_CLK2 trace must be ~17mm less than PC_CLK1. PC_CLK1 trace must be ~17mm less than PC_CLK0.

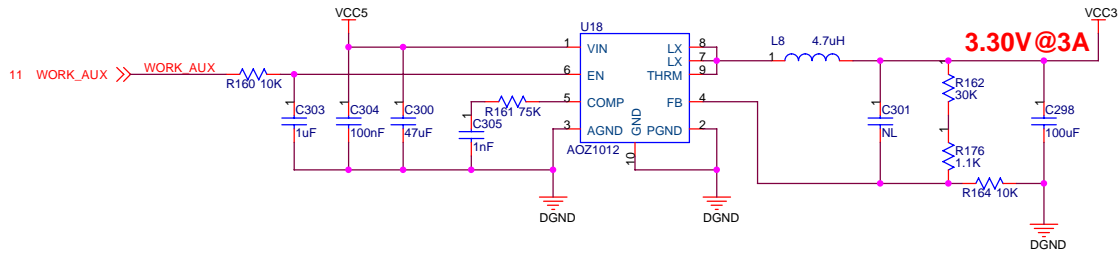
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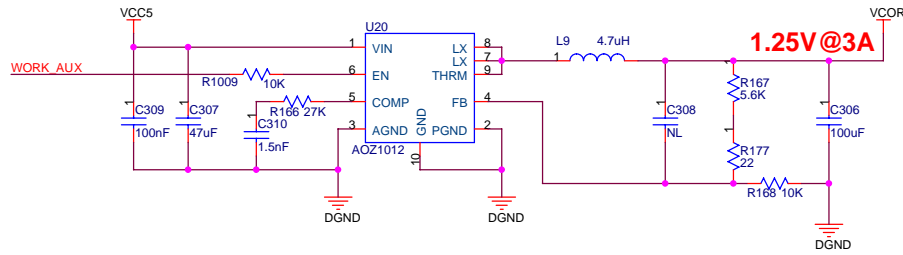
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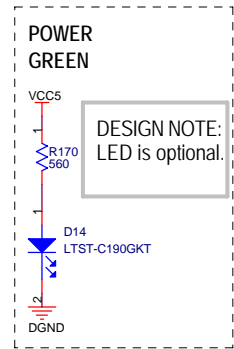
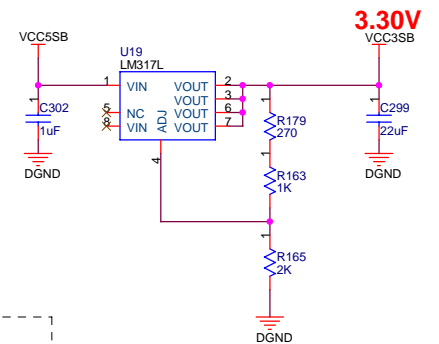
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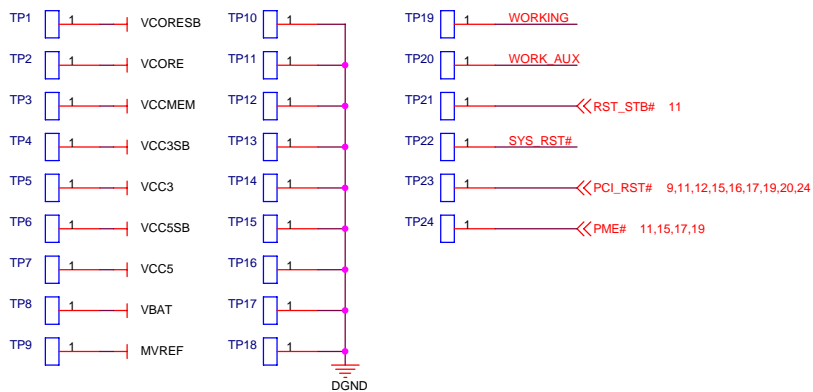
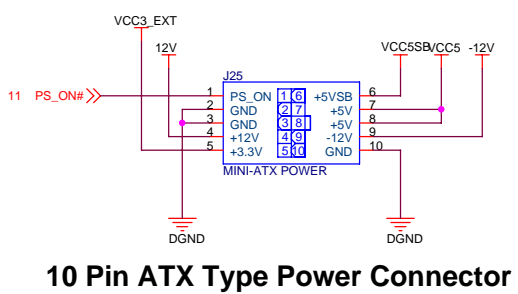
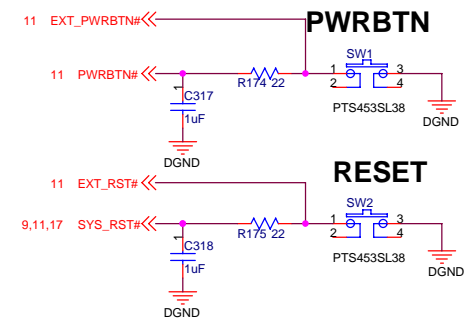
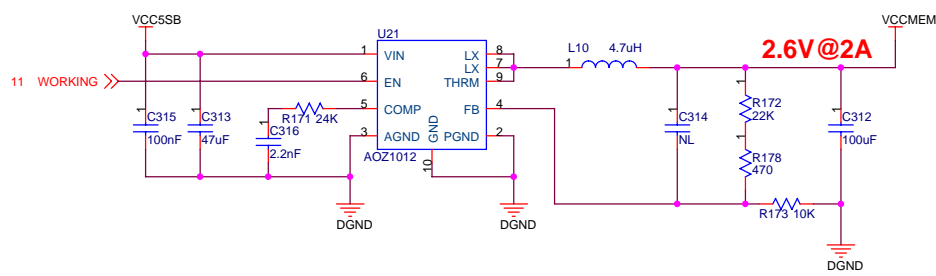
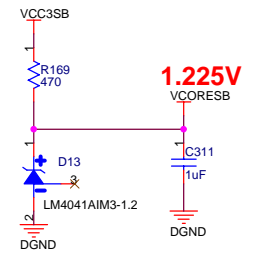
DESIGN NOTE: For TFT support, VCORE must power up before VCC3. With this design, a simple RC is on the enable to the VCC3 regulator delays VCC3 relative to VCORE.



DESIGN NOTE: OPN's for the LX processor have a specified Vcore of 1.25V or 1.20V. If using an OPN that has a Vcore of 1.2V then R3 should be 10K ohms.



DESIGN NOTE: LED is optional.



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